20V-50V bus 120W output series anti-radiation DC/DC converter

1 Product Overview

The input voltage range of the 120W output series anti-radiation DC/DC converter is 20V~50V, and the output voltage includes 3.3V 5V、6.3V、8V、9.5V、12V、15V、20V、28V、±5V、±9.5V、±12V、±15V。

The product adopts single-ended forward excitation and magnetically isolated feedback topology, and the input and output are electrically isolated; The core chip is independently developed; It is manufactured using a thick-film hybrid integration process and is encapsulated in a fully sealed metal case. Dimensions: 76.70mm× 38.60mm×10.66mm. The product implements the YC level in Q/QJA 20085 "General Specification for Hybrid Integrated Circuits for Aerospace", and can be applied to satellites, spacecraft, space stations, etc.

The 120W output series of radiation-resistant DC/DC converters includes 13 varieties, as shown in Table 1.

Table 1 List of 120W output series anti-radiation DC/DC converters

Product name	Input voltage range	Rated output voltage	Rated output current	Rated for delivery Output power	weight
LDCD/(20-50)-3R3-66/SP	20V～50V	Single channel 3.3V, output voltage adjustable	20A	66W	76g±6g
LDCD/(20-50)-5-100/SP	20V～50V	Single 5V, adjustable output voltage	20A	100W	76g±6g
LDCD/(20-50)-6R3-100/SP	20V～50V	Single channel 6.3V, output voltage adjustable	16A	100W	76g±6g
LDCD/(20-50)-8-100/SP	20V～50V	Single 8V, adjustable output voltage	12.5A	100W	76g±6g
LDCD/(20-50)-9R5-110/SP	20V～50V	Single channel 9.5V, output voltage adjustable	11.57A	110W	76g±6g
LDCD/(20-50)-12-120/SP	20V～50V	Single channel 12V, output voltage adjustable	10A	120W	76g±6g
LDCD/(20-50)-15-120/SP	20V～50V	Single channel 15V, output voltage adjustable	8A	120W	76g±6g
LDCD/(20-50)-20-120/SP	20V～50V	Single 20V, output voltage adjustable	6A	120W	76g±6g
LDCD/(20-50)-28-112/SP	20V～50V	Single 28V, adjustable output voltage	4A	112W	76g±6g

20V-50V bus 120W output series anti-radiation

LDCD/(20-50)-5-100/D1	20V～50V	Dual ±5V	10A/10A	100W	76g±6g
LDCD/(20-50)-9R5-110/D1	20V～50V	Dual ± 9.5V	5.79A/5.79 A	110W	76g±6g
LDCD/(20-50)-12-110/D1	20V～50V	Dual ± 12V	4.58A/4.58 A	110W	76g±6g
LDCD/(20-50)-15-120/D1	20V～50V	Dual ± 15V	4A/4A	120W	76g±6g

2 Features:

- Input voltage range: 20V~50V, nominal 28V/42V
- Topology: Single-ended forward structure
- Isolation method: magnetic isolation feedback
- Capacitance between the internal input ground terminal and the housing of the module: 6.8nF/1000V
    - Capacitance between the internal output ground terminal and the housing of the module: 6.8nF/1000V
- It has the function of inhibiting, current sharing, short circuit and recoverable protection
- It has input under-voltage protection function
- Synchronous input and synchronous output functions
- Maximum power density:
    - 44.3W/in3 (LDCD/(20-50)-3R3-66/SP).
    - 67W/in3（LDCD/(20-50)-5-100/SP、LDCD/(20-50)-6R3-100/SP、LDCD/(20-50)-8-100/SP、LDCD/(20-50)- 5-100/D1）
    - 75.2W/in3（LDCD/(20-50)-28-112/SP）
    - 73.8W/in3（LDCD/(20-50)- 12-110/D1、LDCD/(20-50)-12-110/SP 、LDCD/(20-50)-9R5-110/SP、LDCD/(20-50)-9R5-110/D1)
    - 80.5 W/in3 (LDCD/(20-50)-15-120/D1、LDCD/(20-50)-20-120/SP 、LDCD/(20-50)-15-120/SP）
- Operating temperature range (*TC*):-55° C~125° C
- Anti-total dose irradiation: ≥ 100 krad (Si).
- Anti-single event threshold LET: ≥75MeV·cm^2/mg
- Metal-hermetically sealed, hermetically sealed enclosure

3 Conditions of Use

Table 2 Absolute maximum ratings and recommended operating conditions

Absolute maximum rating [note 1].	Input voltage: 19V~51V Output power: 76W （LDCD/(20-50)-3R3-66/SP） 115W（LDCD/(20-50)-5-100/SP） 115W(LDCD/(20-50)-6R3-100/SP) 115W（LDCD/(20-50)-8-100/SP) 126W(LDCD/(20-50)-9R5-110/SP) 126 W(LDCD/(20-50)-12-110/SP) 138W(LDCD/(20-50)-15-120/SP) 138W(LDCD/(20-50)-20-120/SP) 129W(LDCD/(20-50)-28-112/SP) 115W(LDCD/(20-50)-5-100/D1) 126W(LDCD/(20-50)-9R5-110/D1) 126W(LDCD/(20-50)-12-110/D1) 138W(LDCD/(20-50)-15-120/D1) Case operating temperature (*TC*): -55° C~125° C Storage temperature: -65° C~150° C Lead soldering temperature: 300° C (10s). Junction temperature to shell temperature rise: 25° C	Recommended working conditions [Note.] 2]	Input voltage: 20V~50V output power: 3W～66W（LDCD/(20-50)-3R3-66/SP） 5W～100W（LDCD/(20-50)-5-100/SP） 5W～100W（LDCD/(20-50)-6R3-100/SP） 5 W～100W（LDCD/(20-50)-8-100/SP） 5 W～110W（LDCD/(20-50)-9R5-110/SP） 5 W～110W（LDCD/(20-50)-12-120/SP） 6 W～120W（LDCD/(20-50)-15-120/SP） 6 W～120W（LDCD/(20-50)-20-120/SP） 5 W～112W（LDCD/(20-50)-28-112/SP） 5 W～100W（LDCD/(20-50)-5-100/D1） 5 W～110W（LDCD/(20-50)-9R5-110/D1） 5W～110W(LDCD/(20-50)-12-110/D1) 6W～120W(LDCD/(20-50)-15-120/D1) Case operating temperature (*TC*): -55° C~125° C

Note 1: Two or more absolute maximum ratings cannot be applied to a device at the same time. Note 2: The output power should be derated with consideration when in use.

4 Block diagram of the electrical principle

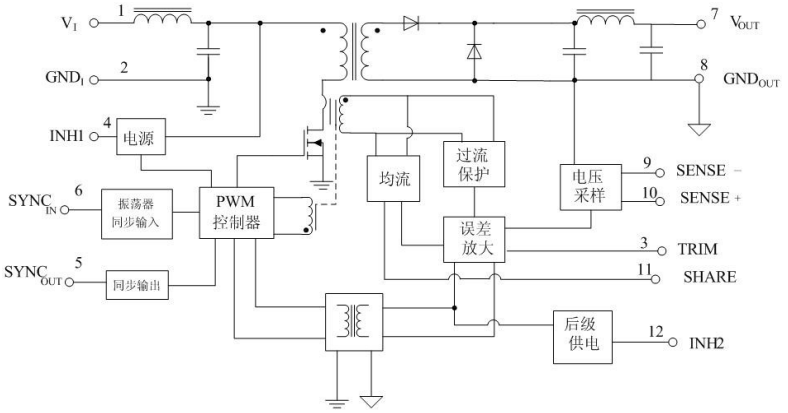


Figure 1(a) is a single-output schematic

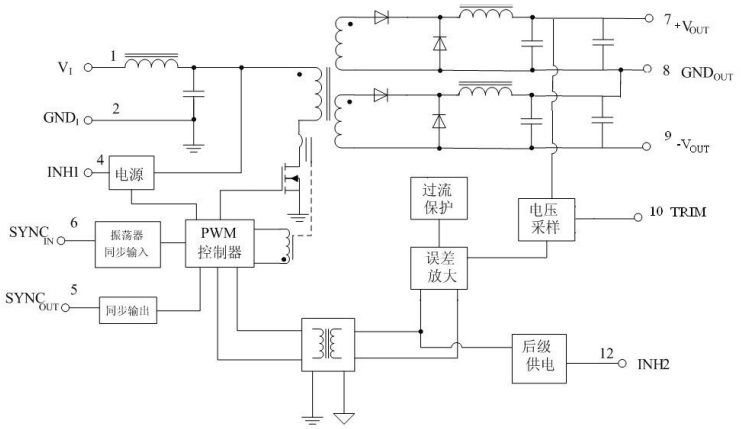


Figure 1(b) is a dual-output schematic

5 Lead-out description

Figure 2 Diagram of the lead end arrangement

Table 3(a) Pinout arrangement (single)

Balloon end number	symbol	name	Balloon end number	symbol	name
1	VI	Enter the positive end	7	VOUT	Output positive end
2	GNDI	Enter the ground terminal	8	GNDOUT	Output ground
3	Trim	Adjust the end	9	SENSE-	The output induces the negative end
4	INH1	Forbidden end 1	10	SENSE+	Outputs the sensing positive end

5	SYNC OUT	Synchronous output	11	SHARE	Current sharing end
6	SYNC IN	Synchronous inputs	12	INH2	Forbidden End 2

Table 3(b) Pinout arrangement (two-way).

Balloon end number	symbol	name	Balloon end number	symbol	name
1	VI	Enter the positive end	7	VO1	Output positive end
2	GNDI	Enter the ground	8	GNDO	Output
3	CASE	Shell ends	9	VO2	Output negative end
4	INH1	Forbidden end 1	10	TRIM	Adjust the end
5	SYNC OUT	Synchronous output	11	NC	Empty end
6	SYNC IN	Synchronous inputs	12	INH2	Forbidden End 2

6 Electrical characteristics of series products

Table 4 LDCD/(20-50)-3R3-66/SP Electrical Characteristics Meter

serial number	characteristic	symbol	condition (Unless otherwise specified, 55 ° C≤ TC≤ 125 ° C, *VI=28V±0.5V* vs. *VI=42V±0.5V*, Prohibit open end, *CL=0*, 6-pin synchronous input termination to ground).	Group A is grouped	Extreme values			unit
					least	typical	utmost	
1	Output voltage	*VO*	*IO=20A*	1	3.25	3.30	3.35	V
				2,3	3.20	3.30	3.40	
2	Output current	*IO*	*VI=20V～50V*	1,2,3	—	20	20	A
3	Output ripple voltage (Peak-Peak).	*VRIP*	BW=10kHz～6MHz, *IO=20A*	1,2,3	—	30	80	mV
4	Voltage regulation	*SV*	*VI=20V→50V*, *IO=20A*	1,2,3	—	3	50	mV
5	Load regulation	*SI*	*IO=0→20A*	1,2,3	—	5	50	mV
6	Input current	*IIN*	Fully loaded, inhibition 1 is connected to the input ground, prohibited End 2 open	1,2,3	—	5.1	14	mA
			Fully loaded, inhibition 2 is connected to the output ground, prohibited End 1 open	1,2,3	—	42	100	
			No-load, open at the forbidden end 1 and forbidden at the forbidden end	1,2,3	—	65	150	

7	Switching frequency [b]	*fs*	*IO* =20A	4,5,6	400	450	600	kHz
8	efficiency	*η*	Input voltage *VI=28V*, *IO*=20A	1	74	78	—	%
				2,3	72	76	—	
			Input voltage *VI=42V*, *IO*=20A	1	72	77	—	
				2,3	70	75	—	
9	Short-circuit power consumption	*PD*	The input voltage *VI=28V*, the output is short-circuited	1,2,3	—	8	20	W
			The input voltage *VI=42V*, the output is short-circuited	1,2,3	—	10	30	
10	Capacitive load ab	*CL*	*VI=28V*, full load	4	—	2000	2000	μF
11	Insulation resistance	*RI*	Between inputs, outputs, and any lead-outs Add 500VDC between the enclosures	1	100	10000	—	MΩ
12	Output voltage change during load jump (peak) [bc]	*VLT*	*VI = 28V*, 42V, 50% load→ full load or full load→ 50% load, 10% load → 50%. Load 50% load → 10% load	4	-500	260	500	mV

serial number	characteristic	symbol	condition (Unless otherwise specified, 55 ° C≤ TC≤ 125 ° C, *VI=28V±0.5V* vs. *VI=42V±0.5V*, Prohibit open end, *CL=0*, 6-pin synchronous input termination to ground).	Group A is grouped	Extreme values			unit
					least	typical	utmost	
13	The recovery time of the output voltage at the time of load jump [bcd]	*tLT*	*VI = 28V*, 42V, 50% load→ full load or full load→ 50% load, 10% load → 50%. Load 50% load → 10% load	4	—	180	500	μs
14	Output voltage change (peak) at input voltage jump [be]	*VVT*	Input voltage *VI*: 23→50V, *IO=20A* Input voltage *VI*: 50→23V, *IO=20A*	4	-500	300	500	mV
15	When the input voltage jumps The recovery time bde of the output voltage	*tVT*	Input voltage *VI*: 23→50V, *IO=20A* Input voltage *VI*: 50→23V, *IO=20A*	4	—	200	500	μs
16	Initiating Overshoot (Peak) [b]	*VTO*	Input voltage *VI:* 0V→28V, 0→42V, *IO* =20A	4,5,6	—	30	160	mV
17	Startup delay [bf]	*tTR*	Input voltage *VI:* 0V→28V, 0→42V, *IO=20A*	4,5,6	—	5	20	ms

18	Load failure recovery time [b]	*tLF*	*IO* from short circuit to 20A	4,5,6	—	2	200	ms
19	Prohibit terminal open-circuit voltage	*VINH*	-	1	—	13	16	V
20	Protection power	*PW*	*IO≥24A*	4	80	80	—	W
21	Enter the reflected ripple current (Peak-Peak).	*IRIP*	BW=20MHz, VI=28V、42V, *IO=20A*, with EMI filter	1	—	50	300	mA
22	Enter the reflected ripple voltage (Peak-Peak).	*VRIP*	BW=20MHz, *IO=20A*, with EMI filter Oscillators	1	—	60	500	mV
23	External synchronization frequency range	*fSYNC*	IO=20A, 6 pins TTL level (VIH≥4.5V, VIL≤0.8V), duty cycle 40%~60%.	4	450	-	550	kHz

[a] capacitive load can be anything between 0 and the maximum limit value;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should not be less than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs ;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground;

table 5LDCD/(20-50)-5-100/SP Electrical Characteristic Meter

serial number	Characteristics	symbol	strip item (Unless otherwise specified, -55° C≤ TC≤ 125° C, *VI=28V±0.5V* vs. *VI*=42V±0.5V, no open end, *CL*=0,6,Pin synchronous input terminal to ground)	Group A is grouped	Extreme values least	typical	utmost	unit
1	Output voltage	*VO*	*IO=20A*	1	4.95	5.00	5.05	V
				2,3	4.90	5.00	5.10	
2	Output current	*IO*	*VI=20V～50V*	1,2,3	-	20	20	A
3	Output ripple voltage (Peak-to-Peak)	*VRIP*	BW=10kHz～6MHz, *IO=20A*	1,2,3	—	40	80	mV
4	Voltage regulation	*SV*	*VI=20V→50V*, *IO=20A*	1,2,3	—	3	50	mV
5	Load regulation	*SI*	*IO=0→20A*	1,2,3	—	5	50	mV
6	Input current	*IIN*	Fully loaded, inhibition 1 is connected to the input ground, prohibited End 2 open	1,2,3	—	5.1	14	mA
			Fully loaded, inhibition 2 is connected to the output ground,	1,2,3	—	42	100	

			prohibited End 1 open					
			No-load, open at the forbidden end 1 and forbidden at the forbidden end	1,2,3	—	65	150	
7	Switching frequency [b]	*fs*	*IO* =20A	4,5,6	400	450	600	kHz
8	efficiency	η	Input voltage *VI=28V*, *IO*=20A	1	80	83	—	%
				2,3	78	81	—	
			Input voltage *VI=42V*, *IO*=20A	1	78	83	—	
				2,3	76	81	—	
9	Short-circuit power consumption	*PD*	The input voltage *VI=28V*, the output is short-circuited	1,2,3	—	8	20	W
			The input voltage *VI=42V*, the output is short-circuited	1,2,3	—	10	30	
10	Capacitive load [ab]	*CL*	*VI=28V*, full load, no for DC steady-state parameters effect	4	—	1000	1000	μF
11	Insulation resistance	*RI*	Between inputs, outputs, and any lead-outs Add 500VDC between the enclosures	1	100	10000	—	MΩ
12	Output voltage change during load jump (peak) [bc]	*VLT*	*VI = 28V*, 42V, 50% load→ full load or full Load → 50% load, 10% load→ 50% load, 50% load→ 10% load	4	-750	300	750	mV
13	The recovery time of the output voltage at the time of load jump [bcd]	*tLT*	*VI = 28V*, 42V, 50% load→ full load or full Load → 50% load, 10% load→ 50% load, 50% load→ 10% load	4	—	200	750	μs
14	Output voltage change (peak) at input voltage jump [be]	*VVT*	Input voltage *VI*: 23→50V, *IO=20A* Input voltage *VI*: 50→23V, *IO=20A*	4	-750	350	750	mV
15	When the input voltage jumps The recovery time bde of the output voltage	*tVT*	Input voltage *VI*: 23→50V, *IO=20A* Input voltage *VI*: 50→23V, *IO=20A*	4	—	300	750	μs
16	Initiating Overshoot (Peak) [b]	*VTO*	Input voltage *VI*: 0V→ 28V, 0→42V, *IO* =20A	4,5,6	—	40	250	mV
17	Startup delay [bf]	*tTR*	Input voltage *VI*: 0V→28V, 0→42V, *IO=20A*	4,5,6	—	5	20	ms
18	Load failure recovery time [b]	*tLF*	*IO* from short circuit to 20A	4,5,6	—	3	200	ms
19	Prohibit terminal open-circuit	*VINH*	-	1	-	13	16	V

	voltage							
20	Protection power	*PW*	-	4	120	120	-	W
21	Input reflected ripple current (peak-to-peak)	*IRIP*	BW=20MHz, VI=28V、42V, *IO=20A*, Connect an EMI filter	1	-	80	300	mA
22	Input reflected ripple electricity Pressure (peak-to-peak)	*VRIP*	BW=20MHz, *IO=20A*, connected to EMI filter	1	-	50	500	mV
23	External synchronization frequency range	*fSYNC*	IO=20A, 6 Pin TTL Level (VIH≥4.5V, VIL≤0.8V), duty cycle 40%~60%	4	450	-	550	kHz

[a] Capacitive load can be anything from 0 to the maximum limit value without affecting DC parameters;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should be greater than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground;

Table 6 LDCD/(20-50)-6R3-100/SP Electrical Characteristics Meter

serial number	Characteristics	symbol	strip item (Unless otherwise specified, 55° C≤ TC≤125° C, *VI=28V±0.5V* vs. *VI*=42V±0.5V, prohibit open end, *CL=0*, 6-pin synchronous input terminal ground).	Group A is grouped	Extreme values			unit
					least	typical	utmost	
1	Output voltage	*VO*	*IO=16A*	1	6.24	6.30	6.36	V
				2,3	6.17	6.30	6.43	
2	Output current	*IO*	*VI=20V～50V*	1,2,3	—	16	16	A
3	Output ripple voltage (Peak-Peak).	*VRIP*	BW=10kHz～6MHz, *IO=16A*	1,2,3	—	50	100	mV
4	Voltage regulation	*SV*	*VI=20V→50V*, *IO=16A*	1,2,3	—	4	63	mV
5	Load regulation	*SI*	*IO=0→16A*	1,2,3	—	5	63	mV
6	Input current	*IIN*	Fully loaded, prohibit terminal 1 to connect to the input ground Prohibition End 2 Open Circuit	1,2,3	—	5.2	14	mA
			Fully loaded, inhibiting terminal 2 to connect to the output ground, Forbidden end 1 is open	1,2,3	—	41	100	
			No-load, open at the forbidden end 1 and forbidden at the	1,2,3	—	75	150	

			forbidden end					
7	Switching frequency b	*fs*	*IO* =16A	4,5,6	400	450	600	kHz
8	efficiency	*η*	Input voltage *VI=28V*, *IO*=16A	1	81	84	—	%
				2,3	79	81	—	
			Input voltage *VI=42V*, *IO*=16A	1	79	83	—	
				2,3	77	80	—	
9	Short-circuit power consumption	*PD*	The input voltage *VI=28V*, the output is short-circuited	1,2,3	—	8	20	W
			The input voltage *VI=42V*, the output is short-circuited	1,2,3	—	10	30	
10	Capacitive load ab	*CL*	*VI=28V*, full load	4	—	2000	2000	μF
11	Insulation resistance	*RI*	Between inputs, outputs, and outlets Add 500VDC between the housing and the housing	1	100	10000	—	MΩ
12	Output voltage change during load jump (peak) bc	*VLT*	*VI = 28V*, 42V, 50% load→ full load or full load→ 50% load, 10% load → 50% load 50% load → 10% load	4	-900	300	900	mV
13	The recovery time of the output voltage at the time of load jump bcd	*tLT*	*VI = 28V*, 42V, 50% load→ full load or full load→ 50% load, 10% load → 50% load 50% load → 10% load	4	—	200	900	μs
14	Output voltage change (peak) at input voltage jump be	*VVT*	Input voltage *VI*: 23→50V, *IO=16A* Input voltage *VI*: 50→23V, *IO=16A*	4	-900	200	900	mV
15	The recovery of the output voltage when the input voltage jumps Time BDE	*tVT*	Input voltage *VI*: 23→50V, *IO=16A* Input voltage *VI*: 50→23V, *IO=16A*	4	—	200	900	μs
16	Initiating Overshoot (Peak) b	*VTO*	Input voltage *VI:* 0V→28V, 0→42V, *IO* =16A	4,5,6	—	50	300	mV
17	Startup delay bf	*tTR*	Input voltage *VI:* 0V→28V, 0→42V, *IO=16A*	4,5,6	—	5	20	ms
18	When the load is recovered B	*tLF*	*IO* from short circuit to 16A	4,5,6	—	2	200	ms
19	Prohibit terminal open-circuit voltage	*VINH*	-	1	—	13	16	V
20	Protection power	*PW*	*IO≥19.2A*	4	120	120	—	W

21	Input reflected ripple current (peak-to-peak).	*IRIP*	BW=20MHz, VI=28V、42V, *IO=16A*, with EMI filter	1	—	50	300	mA
22	Input reflected ripple voltage (peak-to-peak).	*VRIP*	BW=20MHz, *IO=16A*, connected to EMI filter	1	—	40	500	mV
23	External synchronization frequency range	*fSYNC*	IO=16A, 6 pins TTL level (VIH≥4.5V, VIL≤0.8V), duty cycle 40%~60%.	4	450	-	550	kHz

[a] capacitive load can be anything between 0 and the maximum limit value;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should not be less than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs ;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground;

Table 7 LDCD/(20-50)-8-100/SP Electrical Characteristic Meter

serial nu	Characteri	symbo	strip item (Unless otherwise -55° C≤ TC≤125° C, *VI=28V±1V* with	Group grouping	pol lim value e it			unit
					least	typical	utmost	
1	Output	*VO1*	*IO* =12.5A	1	7.92	8.00	8.08	V
				2,3	7.82	8.00	8.18	
2	Output current	*IO1*	*VI=20V～50V*	1,2,3	—	12.5	12.5	A
3	Output ripple voltage (Peak-to-Peak)	*VR1*	BW=10kHz～6MHz, *VI=28V*、*IO=12.5A*	1	—	40	150	mV
				2,3		50	200	
4	Voltage regulation	*SV1*	*VI=20V→50V*, *IO* =12.5A	1,2,3	—	5	80	mV
5	Load regulation	*SI1*	*IO* =0→12.5A	1,2,3	—	5	80	mV
6	Input current	*IIN*	Fully loaded, the forbidden end 1 is connected to the input ground terminal, the forbidden terminal 2 Open Circuit	1,2,3	—	5.2	10	mA
			Fully loaded, the forbidden terminal 2 is connected to the output ground terminal, the forbidden terminal 1 Open Circuit		—	44	100	

			No load, open at the forbidden end 1 and open at the forbidden end 2		—	50	130	
7	Switching frequency [b]	*fs*	*VI*=28V±1V, *IO* =12.5A	4,5,6	400	450	600	kHz
8	efficiency	*η*	Input voltage *VI*=28V *IO*=12.5A	1	82	85.0	—	%
				2, 3	80	83.5	—	
			Input voltage *VI*=42V *IO*=12.5A	1	81	84.5	—	
				2, 3	79	83.0	—	
9	Short-circuit power consumption	*PD*	*VI*=28V, output short circuit	1,2,3	—	8.5	30	W
			VI=42V, output short circuit	1,2,3	—	10.4	40	
10	Capacitive load [ab]	*CL*	*VI*=28V, no effect on DC steady-state parameters	4	—	2000	2000	μF
11	Insulation resistance	*RISO*	Add 500V DC between the inputs, outputs, and between either pinout and housing (except for the 11th terminal).	1	100	10000	—	MΩ
12	The output voltage changes BC during load jumps (Peak)	*VLOR*	*VI*=28V, 42V, 50% load→ full load or full load → 50% load, 10% load→ 50% load Load → 10% load	4	-800	150	800	mV
13	The recovery of the output voltage during load jumps Time [BCD]	*tLOR*	*VI*=28V, 42V, 50% load→ full load or full load → 50% load, 10% load→ 50% load Load → 10% load	4	—	0.2	1	ms
14	When the input voltage jumps Output voltage change (peak) [be]	*VVOR*	Input voltage *VI*: 23V→50V, *IO*=12.5A	4	-800	300	800	mV
15	The output voltage at the time of the input voltage jump Recovery time [BDE]	*tVOR*			-	0.25	1	ms
16	Start the overshoot (peak) [b]	*VTO*	Input voltage *VI*=0→28V, *IO*=12.5A	4,5,6	—	50	400	mV
			Input voltage *VI*=0→42V, *IO*=12.5A	4,5,6	—	50	400	mV
17	Startup delay f	*tTR*	Input voltage *VI*=0→28V, *IO*=12.5A	4,5,6	—	5.0	25	ms
			Input voltage *VI*=0→42V, *IO*=12.5A	4,5,6	—	5.0	25	ms
18	Load failure recovery time [bd]	*tLF*	*VI*=28V±1V, IO from short to 12.5A	4	—	2.0	300	ms

19	Protection power	*PW*	*IO≥14.37A*	4	115	115	-	W
20	It is forbidden to open the circuit at the end press	*VINH*	-	1	-	13.0	16	V
21	Input reflected ripple current (peak-to-peak).	*IRIP*	BW=10kHz～6MHz, VI=28V、42V, *IO=11.57A*, with EMI filter	1	-	60	300	mA
22	Input reflected ripple voltage (peak-to-peak).	*VRIP*	BW=10kHz~6MHz, *IO=11.57A*, connected to EMI filter	1	-	70	500	mV
23	External synchronization frequency	*f*	*VI=28V±1V*, *IO*=12.5A, 6 pins to TTL Level (*VIH≥ 4.5V*, *VIL≤0.8V*, duty cycle 40%～60%)	4	450	-	550	kHz

[a] Capacitive load can be anything from 0 to the maximum limit value without affecting DC parameters;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should be greater than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground.

Table 8 LDCD/(20-50)-9R5-110/SP electrical characterization meter

serial number	Characteristics	symbol	Conditions (Unless otherwise specified, -55° C≤ TC≤125° C, VI=28V±1V & VI=42V±1V, No Open End, CL=0)	Group As grouped	possible limit value least	Typical	utmost	unit
1	Output voltage	*VO1*	*IO* =11.57A	1	9.40	9.5	9.60	V
				2,3	9.30	9.5	9.70	
2	Output current	*IO1*	*VI=20V～50V*	1,2,3	—	11.57	11.57	A
3	Output ripple voltage (Peak-to-Peak)	*VR1*	BW=10kHz～6MHz, *VI=28V*、42V, *IO=11.57A*	1	—	45	150	mV
				2,3		60	200	
4	Voltage regulation	*SV1*	*VI=20V→50V*, *IO* =11.57A	1,2,3	—	5	100	mV
5	Load regulation	*SI1*	*IO* =0→11.57A	1,2,3	—	10	150	mV

6	Input current	*IIN*	Fully loaded, inhibition 1 is connected to the input ground, prohibited End 2 is open	1,2,3	—	5.3	10	mA
			Fully loaded, inhibition 2 is connected to the output ground, prohibited End 1 is open		—	55	100	
			No load, open at the forbidden end 1 and open at the forbidden end 2		—	60	130	
7	Switching frequency [b]	*fs*	*VI*=28V±1V, *IO* =11.57A	4,5,6	400	450	600	kHz
8	efficiency	*η*	Input voltage *VI*=28V I_0=11.57A	1	83	85.5	—	%
				2, 3	81	84.0	—	
			Input voltage *VI*=42V *IO*=11.57A	1	82	85.0	—	
				2, 3	80	83.5	—	
9	Short-circuit power consumption	*PD*	*VI*=28V, output short circuit	1,2,3	—	8.5	30	W
			VI=42V, output short circuit	1,2,3	—	10.5	40	
10	Capacitive load [ab]	*CL*	*VI*=28V, no effect on DC steady-state parameters	4	—	2000	2000	μF
11	Insulation resistance	*RISO*	Add 500V DC between the inputs, outputs, and between either pinout and housing (except for the 11th terminal).	1	100	10000	—	MΩ
12	The output voltage changes BC during load transitions (Peak)	*VLOR*	*VI* = 28V, 42V, 50% load→ full load or full load→ 50% load, 10% load→ 50% load 50% load → 10% load	4	-950	250	950	mV
13	Lose when the load jumps The recovery time of the output voltage is bcd	*tLOR*	*VI* = 28V, 42V, 50% load→ full load or full load→ 50% load, 10% load→ 50% load 50% load → 10% load	4	—	0.2	1	ms
14	The output voltage changes when the input voltage jumps (Peak) [be]	*VVOR*	Input voltage *VI*: 23V→50V, *IO*=11.57A	4	-950	600	950	mV
15	The recovery time BDE of the output voltage when the input voltage jumps	*tVOR*			-	0.2	1	ms
16	Start the overshoot (peak) [b]	*VTO*	Input voltage *VI*=0→28V, *IO*=11.57A	4,5,6	—	70	475	mV
			Input voltage *VI*=0→42V, *IO*=11.57A	4,5,6	—	70	475	mV

17	Startup delay [f]	*tTR*	Input voltage *VI*=0→28V, *IO=11.57A*	4,5,6	—	5	25	ms
			Input voltage *VI*=0→42V, *IO=11.57A*	4,5,6	—	5	25	ms
18	Load failure recovery time bd	*tLF*	*VI=28V±1V*, IO from shorted to 11.57A	4	—	2.0	300	ms
19	Protection power	*PW*	*IO≥13.3A*	4	126	126	-	W
20	It is forbidden to open the circuit at the end press	*VINH*	-	1	-	13.0	16	V
21	Input reflected ripple current (peak-to-peak).	*IRIP*	BW=10kHz～6MHz, VI=28V、42V, *IO=11.57A*, with EMI filter	1	-	60	300	mA
22	Input reflected ripple voltage (peak-to-peak).	*VRIP*	BW=10kHz~6MHz, *IO=11.57A*, connected to EMI filter	1	-	80	500	mV
23	External synchronization frequency	*f*	*VI=28V±1V*, *IO*=11.57A, 6 pins to TTL Level (*VIH≥ 4.5V*, *VIL≤0.8V*, duty cycle 40%～60%)	4	450	-	550	kHz

[a] Capacitive load can be anything from 0 to the maximum limit value without affecting DC parameters;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should be greater than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground

Table 9 LDCD/(20-50)-12-120/SP Electrical Characteristic Meter

serial number	characteristic	symbol	condition (-55 ° C≤ TC≤ 125 ° C unless otherwise specified *VI=28V±1V* vs. *VI=42V±0.5V*, Prohibit open end, *CL=0*, 6-pin synchronous input termination to ground).	Group A is grouped	Extreme values			unit
					least	typical	utmost	
1	Output voltage	*VO*	*IO=10A*	1	11.88	12.000	12.12	V
				2,3	11.64	12.000	12.36	
2	Output current	*IO*	*VI=20V～50V*	1,2,3	-	10	10	A
3	Output ripple voltage	*VRIP*	BW=10kHz～6MHz, *IO=10A*	1	—	75	120	mV
				2,3	—	100	150	

	(Peak-Peak).							
4	Voltage regulation	*SV*	*VI=20V→50V, IO=10A*	1,2,3	—	10	120	mV
5	Load regulation	*SI*	*IO=0→10A*	1,2,3	—	10	120	mV
6	Input current	*IIN*	Fully loaded, inhibition 1 is connected to the input ground, prohibited End 2 open	1,2,3	—	7.5	10	mA
			Fully loaded, inhibition 2 is connected to the output ground, prohibited End 1 open	1,2,3	—	70	100	
			No-load, open at the forbidden end 1 and forbidden at the forbidden end	1,2,3	—	75	130	
7	Switching frequency [b]	*fs*	*IO* =10A	4,5,6	400	450	600	kHz
8	efficiency	*η*	Input voltage *VI=28V, IO*=10A	1	83	85.0	—	%
				2,3	81	83.0	—	
			Input voltage *VI=42V, IO*=10A	1	82	85.3	—	
				2,3	80	83.4	—	
9	Short-circuit power consumption	*PD*	The input voltage *VI=28V*, the output is short-circuited	1,2,3	—	4	30	W
			The input voltage *VI=42V*, the output is short-circuited	1,2,3	—	6	40	
10	Capacitive load [ab]	*CL*	*VI=28V*, full load	4	—	470	470	μF
11	Insulation resistance	*RI*	Between inputs, outputs, and any lead-outs Add 500VDC between the enclosures	1	100	30000	—	MΩ
12	The output voltage changes (peak) BC during load jump	*VLT*	*VI = 28V*, 42V, 50% load→ full load or full load→ 50% load, 10% load → 50% load 50% load → 10% load	4	-1200	400	1200	mV
13	The recovery time bcd of the output voltage at the time of the load jump	*tLT*	*VI = 28V*, 42V, 50% load→ full load or full load→ 50% load, 10% load → 50% load 50% load → 10% load	4	—	0.2	1	ms
14	Input voltage jump when the output voltage	*VVT*	Input voltage *VI*: 23→50V, *IO=10A* Input voltage *VI:* 50→23V, *IO=10A*	4	-1200	600	1200	mV

	changes (peak) [be]							
15	When the output voltage is restored when the input voltage jumps between [bde]	*tVT*	Input voltage *VI*: 23→50V, *IO=10A* Input voltage *VI*: 50→23V, *IO=10A*	4	—	0.2	1	ms
16	Start the overshoot (Peak) [b]	*VTO*	Input voltage *VI*: 0V→28V, 0→42V, *IO* =10A	4,5,6	—	0	600	mV
17	Startup delay [bf]	*tTR*	Input voltage *VI*: 0V→28V, 0→42V, *IO=10A*	4,5,6	—	6	20	ms
18	Load failure recovery Complex time b	*tLF*	*IO* from short circuit to 10A	4,5,6	—	4	300	ms
19	Prohibit terminal open-circuit voltage	*VINH*	-	1	-	13	16	V
20	Protection power	*PW*	*IO≥10.6A*	4	126.5	126.5	-	W
21	Input reflected ripple current (peak-to-peak).	*IRIP*	BW=20MHz, VI=28V、42V, *IO=10A*, Connect an EMI filter	1	-	120	300	mA
22	Input reflected ripple voltage (peak-to-peak).	*VRIP*	BW=20MHz, *IO=10A*, with EMI filtering utensil	1	-	100	500	mV
23	External synchronization frequency range	*fSYNC*	IO=10A, 6 pins TTL level (VIH≥4.5V, VIL≤0.8V), duty cycle 40%~60%.	4	450	-	550	kHz

[a] capacitive load can be anything between 0 and the maximum limit value;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should not be less than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs ;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground;

Table 10 LDCD/(20-50)-15-120/SP Electrical Characteristics Meter

serial number	characteristic	symbol	condition (-55 ° C≤ TC≤ 125 ° C unless otherwise specified *VI=28V±1V* vs. *VI=42V±0.5V*, Prohibit open end, *CL=0*, 6-pin synchronous input termination to ground).	Group A is grouped	Extreme values			unit
					least	typical	utmost	
1	Output voltage	*VO*	*IO=8A*	1	14.85	15.000	15.15	V
				2,3	14.55	15.000	15.45	
2	Output current	*IO*	*VI=20V～50V*	1,2,3	—	8	8	A
3	Output ripple voltage (Peak-Peak).	*VRIP*	BW=10kHz～6MHz, *IO=8A*	1	—	75	150	mV
				2,3	—	100	200	
4	Voltage regulation	*SV*	*VI=20V→50V*, *IO=8A*	1,2,3	—	10	150	mV
5	Load regulation	*SI*	*IO=0→8A*	1,2,3	—	10	150	mV
6	Input current	*IIN*	Fully loaded, inhibition 1 is connected to the input ground, prohibited End 2 open	1,2,3	—	7.5	10	mA
			Fully loaded, inhibition 2 is connected to the output ground, prohibited End 1 open	1,2,3	—	70	100	
			No-load, open at the forbidden end 1 and forbidden at the forbidden end	1,2,3	—	65	130	
7	Switching frequency [b]	*fs*	*IO* =8A	4,5,6	400	450	600	kHz
8	efficiency	*η*	Input voltage *VI=28V*, *IO*=8A	1	84	85.5	—	%
				2,3	82	83.0	—	
			Input voltage *VI=42V*, *IO*=8A	1	83	85.7	—	
				2,3	81	83.5	—	
9	Short-circuit power consumption	*PD*	The input voltage *VI=28V*, the output is short-circuited	1,2,3	—	4	30	W
			The input voltage *VI=42V*, the output is short-circuited	1,2,3	—	6	40	
10	Capacitive load [ab]	*CL*	*VI=28V*, full load	4	—	470	470	μF
11	Insulation resistance	*RI*	Between inputs, outputs, and any lead-outs Add 500VDC between the enclosures	1	100	30000	—	MΩ
12	Output voltage change during load jump (peak to peak)	*VLT*	*VI = 28V*, 42V, 50% load→ full load or full load→ 50% load, 10% load → 50%.	4	-1500	700	1500	mV

			Load 50% load → 10% load					
13	The recovery time of the output voltage at the time of load jump bcd	*tLT*	*VI = 28V*, 42V, 50% load→ full load or full load→ 50% load, 10% load → 50%. Load 50% load → 10% load	4	—	0.2	1	ms
14	Output voltage change (peak) at input voltage jump be	*VVT*	Input voltage *VI*: 23→50V, *IO=8A* Input voltage *VI*: 50→23V, *IO=8A*	4	-1500	600	1500	mV
15	When the input voltage jumps The recovery time bde of the output voltage	*tVT*	Input voltage *VI*: 23→50V, *IO=8A* Input voltage *VI*: 50→23V, *IO=8A*	4	—	0.2	1	ms
16	Initiating Overshoot (Peak) b	*VTO*	Input voltage *VI:* 0V→28V, 0→42V, *IO* =8A	4,5,6	—	0	750	mV
17	Startup delay bf	*tTR*	Input voltage *VI:* 0V→28V, 0→42V, *IO=8A*	4,5,6	—	6	20	ms
18	Load failure recovery time b	*tLF*	*IO* from short circuit to 8A	4,5,6	—	6	300	ms
19	Prohibit terminal open-circuit voltage	*VINH*	-	1	-	13	16	V
20	Protection power	*PW*	*IO≥9.2A*	4	138	138	-	W
21	Input reflected ripple current (peak-to-peak).	*IRIP*	BW=20MHz, VI=28V、42V, *IO=8A*, with EMI filter	1	-	100	300	mA
22	Input reflected ripple voltage (peak-to-peak).	*VRIP*	BW=20MHz, *IO=8A*, with EMI filtering utensil	1	-	100	500	mV
23	External synchronization frequency range	*fSYNC*	IO=8A, 6 pins TTL level (VIH≥4.5V, VIL≤0.8V), duty cycle 40%~60%.	4	450	-	550	kHz

[a] capacitive load can be anything between 0 and the maximum limit value;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should not be less than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs ;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground;

Table 11 LDCD/(20-50)-20-120/SP Electrical Characteristics Meter

serial number	characteristic	symbol	condition (-55 ° C≤ TC≤ 125 ° C unless otherwise specified *VI=28V±1V* vs. *VI=42V±0.5V*, Prohibit open end, *CL=0*, 6-pin synchronous input termination to ground).	Group A is grouped	Extreme values			unit
					least	typical	utmost	
1	Output voltage	*VO*	*IO=6A*	1	19.8	20.01	20.2	V
				2,3	19.6	19.96	20.4	
2	Output current	*IO*	*VI=20V～50V*	1,2,3	-	6	6	A
3	Output ripple voltage (Peak-Peak).	*VRIP*	BW=10kHz～6MHz, *IO=6A*	1	-	120	200	mV
				2,3	-	150	300	
4	Voltage regulation	*SV*	*VI=20V→50V*, *IO=6A*	1,2,3	—	20	200	mV
5	Load regulation	*SI*	*IO=0→6A*	1,2,3	—	40	200	mV
6	Input current	*IIN*	Fully loaded, inhibition 1 is connected to the input ground, prohibited End 2 open	1,2,3	—	5.0	10	mA
			Fully loaded, inhibition 2 is connected to the output ground, prohibited End 1 open	1,2,3	—	42	100	
			No-load, open at the forbidden end 1 and forbidden at the forbidden end	1,2,3	—	60	130	
7	Switching frequency [b]	*fs*	*IO* =6A	4,5,6	400	450	600	kHz
8	efficiency	*η*	Input voltage *VI=28V*, *IO*=6A	1	84	86	—	%
				2,3	82	85.5	—	
			Input voltage *VI=42V*, *IO*=6A	1	83	84	—	
				2,3	81	83.5	—	
9	Short-circuit power consumption	*PD*	The input voltage *VI=28V*, the output is short-circuited	1,2,3	—	15	30	W
			The input voltage *VI=42V*, the output is short-circuited	1,2,3	—	18	40	

10	Capacitive load [ab]	*CL*	*VI=28V*, full load	4	—	1000	1000	μF
11	Insulation resistance	*RI*	Between inputs, outputs, and any lead-outs Add 500VDC between the enclosures	1	100	40000	—	MΩ
12	The output voltage changes (peak) BC during load jump	*VLT*	*VI = 28V*, 42V, 50% load→ full load or full load→ 50% load, 10% load → 50%. Load 50% load → 10% load	4	-1600	700	1600	mV
13	The recovery time bcd of the output voltage at the time of the load jump	*tLT*	*VI = 28V*, 42V, 50% load→ full load or full load→ 50% load, 10% load → 50%. Load 50% load → 10% load	4	—	0.3	1	ms
14	When the input voltage jumps Output voltage change (peak) [be]	*VVT*	Input voltage *VI:* 23→50V, *IO=6A* Input voltage *VI*: 50→23V, *IO=6A*	4	-1600	1200	1600	mV
15	The output voltage at the time of the input voltage jump Recovery time [BDE]	*tVT*	Input voltage *VI:* 23→50V, *IO=6A* Input voltage *VI*: 50→23V, *IO=6A*	4	—	0.4	1	ms
16	Start the overshoot (peak) [b]	*VTO*	Input voltage *VI:* 0V→28V, 0→42V, *IO* =6A	4,5,6	—	0	1000	mV
17	Startup delay [bf]	*tTR*	Input voltage *VI:* 0V→28V, 0→42V, *IO=6A*	4,5,6	—	5	20	ms
18	Load failure recovery time [b]	*tLF*	*IO* from short circuit to 20A	4,5,6	—	2.2	300	ms
19	It is forbidden to open the circuit at the end press	*VINH*	-	1	-	12.5	16	V
20	Protection power	*PW*	*IO≥6.9A*	4	138	138	-	W
21	Input reflected ripple current (peak-to-peak).	*IRIP*	BW=10kHz～6MHz, VI=28V、42V, *IO=6A*, with EMI filter	1	-	70	300	mA
22	Input reflected ripple voltage	*VRIP*	BW=10kHz～6MHz, *IO=6A*, Connect an EMI filter	1	-	80	500	mV

	(peak-to-peak).							
23	External synchronization frequency range surround	*fSYNC*	IO=6A, 6 pins TTL level (VIH≥4.5V, VIL≤0.8V), duty cycle 40%~60%.	4	450	-	550	kHz

[a] capacitive load can be anything between 0 and the maximum limit value;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should not be less than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs ;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground;

table 12 LDCD/(20-50)-28-112/SP Electrical Characteristic Meter

serial number	characteristic	symbol	condition (-55 ° C≤ TC≤ 125 ° C unless otherwise specified *VI=28V±1V* vs. *VI=42V±0.5V*, Prohibit open end, *CL=0*, 6-pin synchronous input termination to ground).	Group A is grouped	Extreme values least	typical	utmost	unit
1	Output voltage	*VO*	*IO=4A*	1	27.72	28.00	28.28	V
				2,3	27.50	28.00	28.50	
2	Output current	*IO*	*VI=20V～50V*	1,2,3	-	4	4	A
3	Output ripple voltage (Peak-Peak).	*VRIP*	BW=10kHz～6MHz, *IO=4A*	1	—	40	200	mV
				2,3	—	60	300	
4	Voltage regulation	*SV*	*VI=20V→50V*, *IO=4A*	1,2,3	—	0.1	1	%
5	Load regulation	*SI*	*IO=0→4A*	1,2,3	—	0.5	1	%
6	Input current	*IIN*	Fully loaded, inhibition 1 is connected to the input ground, prohibited End 2 open	1,2,3	—	5.0	10	mA
			Fully loaded, inhibition 2 is connected to the output ground, prohibited End 1 open	1,2,3	—	45	100	
			No-load, open at the forbidden end 1 and forbidden at the forbidden end	1,2,3	—	50	130	
7	Switching frequency [b]	*fs*	*IO* =4A	4,5,6	400	450	600	kHz
8	efficiency	*η*	Input voltage *VI=28V*, *IO*=4A	1	84	86.4	—	%
				2,3	82	84.2	—	
			Input voltage *VI=42V*, *IO*=4A	1	82	85.3	—	

				2,3	80	83.0	—	
9	Short-circuit power consumption	*PD*	The input voltage *VI=28V*, the output is short-circuited	1,2,3	—	8.0	30	W
			The input voltage *VI=42V*, the output is short-circuited	1,2,3	—	11.2	40	
10	Capacitive load [ab]	*CL*	*VI=28V*, full load	4	—	2000	2000	μF
11	Insulation resistance	*RI*	Between inputs, outputs, and any lead-outs Add 500VDC between the enclosures	1	100	10000	—	MΩ
12	The output voltage changes (peak) BC during load jump	*VLT*	*VI = 28V*, 42V, 50% load→ full load or full load→ 50% load, 10% load → 50%. Load 50% load → 10% load	4	-2240	800	2240	mV
13	The recovery time bcd of the output voltage at the time of the load jump	*tLT*	*VI = 28V*, 42V, 50% load→ full load or full load→ 50% load, 10% load → 50%. Load 50% load → 10% load	4	—	0.2	1	ms
14	When the input voltage jumps Output voltage change (peak) [be]	*VVT*	Input voltage *VI*: 23→50V, *IO=4A* Input voltage *VI*: 50→23V, *IO=4A*	4	-2800	1440	2800	mV
15	Input voltage jump The recovery time of the output voltage bde	*tVT*	Input voltage *VI*: 23→50V, *IO=4A* Input voltage *VI*: 50→23V, *IO=4A*	4	—	0.28	1	ms
16	Start the overshoot (peak) [b]	*VTO*	Input voltage *VI:* 0V→28V, 0→42V, *IO* =4A	4,5,6	—	500	1680	mV
17	Startup delay [bf]	*tTR*	Input voltage *VI:* 0V→28V, 0→42V, *IO=4A*	4,5,6	—	5.0	25	ms
18	Load failure recovery Time [b]	*tLF*	*IO* from short circuit to 4A	4,5,6	—	2.6	300	ms
19	Prohibit terminal open-circuit voltage	*VINH*	-	1	-	13.0	16	V
20	Protection power	*PW*	*IO≥4.6A*	4	128.8	128.8	-	W
21	Input reflected ripple current	*IRIP*	BW=20MHz, VI=28V、42V, *IO=4A*, with EMI filter	1	-	60	300	mA

	(peak-to-peak).							
22	Input reflected ripple voltage (peak-to-peak).	*VRIP*	BW=20MHz, *IO=4A*, connected to EMI filter Oscillators	1	-	70	500	mV
23	External synchronization frequency range	*fSYNC*	IO=4A, 6 pins with TTL level (VIH≥4.5V, VIL≤0.8V), duty cycle 40%~60%.	4	450	-	550	kHz

[a] capacitive load can be anything between 0 and the maximum limit value;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should not be less than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs ;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground;

table 13 LDCD/(20-50)-5-100/D1 Electrical Characteristic Meter

serial number	characteristic	symbol	condition (-55 ° C≤ TC≤ 125 ° C unless otherwise specified *VI=28V±1V* vs. *VI=42V±0.5V*, Prohibit open end, *CL=0*, 6-pin synchronous input termination to ground).	Group A is grouped	Extreme values least	Typical	utmost	unit
1	Output voltage	*VO1*	*IO1=IO2=10A*	1	4.95	5.02	5.05	V
				2,3	4.90	5.01	5.10	
		VO2		1	-5.08	-5.03	-4.92	
				2,3	-5.15	-5.04	-4.85	
2	Output current	*IO1*、*IO2*	*VI=20V～50V*	1,2,3	-	10	10	A
3	Output ripple voltage (Peak-to-Peak)	*VR1*、*VR2*	BW=10KH～6MHz, *IO1=IO2=10A*	1,2,3	—	60	150	mV
4	Voltage regulation	*SV1*	*VI=20V→50V*, *Io1=IO2=10A*	1,2,3	-	10	100	mV
		SV2		1,2,3	-	15	150	
5	Load regulation	*SI1*	*Io1=IO2=0.1A→10A*	1,2,3	—	10	150	mV
		SI2			-	30	200	
6	Input	*IIN*	When fully loaded, the pre-stop end is connected to the input	1,2,3	—	6	10	mA

	current		ground terminal					
			When fully loaded, the rear stop end is connected to the input ground end		-	60	100	
			No load, no end open road		—	50	130	
7	Switching frequency [b]	*fs*	*Io1=IO2=10A*	4,5,6	400	450	600	kHz
8	effi cien cy	*η*	*Vin=28V, Io1=IO2=10A*	1	80	83	—	%
				2,3	78	82	-	
			Vin=42V, Io1=IO2=10A	1	78	82	—	
				2,3	76	81	-	
9	Short-circuit power consumption	*PD*	*Vin=28V,* output short circuit	1,2,3	—	6	30	W
			Vin = 42V, output short circuit		-	8	40	
10	Capacitive load [ab]	*CL1* 、 *CL2*	There is no effect on DC steady-state parameters	4	—	2000	2000	μF
11	Insulation resistance	*RISO*	Add 500VDC between the inputs, outputs, and between either pinout and housing	1	100	3000	—	MΩ
12	Output voltage change during load jump (peak) [bc]	*VLOR*	50% loaded→ full load or, full load → 50% load; 10% loaded→ 50% full, 50% loaded→ 10% full	4	-500	200	500	mV
13	The recovery time of the output voltage at the time of load jump [bcd]	*tLOR*		4	—	0.3	1	ms
14	Output voltage change (peak) at input voltage jump [be]	*VVOR*	Input voltage VI: 23→50V, *Io1=IO2=10A* Input voltage VI: 50→23V, *Io1=IO2=10A*	4	-500	200	500	mV
15	The recovery time of the output voltage at the time of the input transition [bde]	*tVOR*		4	—	0.3	1	ms
16	Initiating Overshoot (Peak) [b]	*VTO*	Input voltage VI: = 0V→ 28V, 0V→ 42V *Io1=IO2=10A*	4,5,6	—	0	250	mV
17	Startup delay [bf]	*tTR*	Input voltage *VI:* 0→28V, 0V→ 42V *Io1 = IO2* =10A	4,5,6	—	5	20	ms

18	Prohibit terminal open-circuit voltage	*VINH*	Forbidden end open circuit, *VI=28V*, 42V, *IO1=IO2=10A*	1	-	13	16	V
19	Protection power	*PW*	*IO1=IO2≥11.5A*	1	115	115	-	W
20	Input reflected ripple current (peak-to-peak).	*IRIP*	BW=10kHz~6MHz, VI=28V, 42V, *Io1=IO2=10A*, with EMI filter Oscillators	1	-	80	300	mA
21	Input reflected ripple voltage (peak-to-peak).	*VRIP*	BW=10kHz～6MHz, *Io1=IO2=10A*, Connect to an EMI filter	1	-	120	500	mV
22	Load failure recovery time	*tLF*	*IO* from short circuit to 10A	4	—	3	300	ms
23	Cross adjustment degree	*SC*	70% load all the way, 30% to 70% load variation all the way	1,2,3	-	3.5	6	%
24	External synchronization frequency range	*fSYNC*	*IO1=IO2=10A*, 6 pins TTL level (VIH≥4.5V, VIL≤0.8V), duty cycle 40%~60%	4,5,6	450	-	550	kHz

[a] Capacitive load can be anything from 0 to the maximum limit value without affecting DC parameters;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should be greater than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground.

table 14 LDCD/(20-50)-9R5-110/D1 Electrical Characteristic Meter

serial number	characteristic	symbol	condition (-55 ° C≤ TC≤ 125 ° C unless otherwise specified *VI=28V±1V* vs. *VI=42V±0.5V*, Prohibit open end, *CL=0*, 6-pin synchronous input termination to ground).	Group A is grouped	Extreme values least	typical	utmost	unit
1	Output voltage	*VO1*	*Io1=IO2=5.79A*	1	9.40	9.50	9.60	V
				2,3	9.31	9.55	9.69	
		VO2		1	-9.65	-9.50	-9.35	
				2,3	-9.74	-9.49	-9.26	
2	Output	*IO1*、	*VI=20V～50V*	1,2,3	-	5.79	5.79	A

	current	*IO2*						
3	Output ripple voltage (Peak-to-Peak)	*VR1*、*VR2*	BW=10KH～6MHz, *IO1=IO2=5.79A*	1,2,3	—	80	150	mV
4	Voltage regulation	*SV1*	*VI=20V→50V*, *Io1=IO2=5.79A*	1,2,3	-	20	100	mV
		SV2		1,2,3	-	20	200	
5	Load regulation	*SI1*	*Io1=IO2=0.06A→5.79A*	1,2,3	—	15	150	mV
		SI2			-	40	200	
6	Input current	*IIN*	When fully loaded, the pre-stop end is connected to the input ground terminal	1,2,3	—	7	10	mA
			When fully loaded, the rear stop end is connected to the input ground end		-	60	100	
			No load, no end open road		—	50	130	
7	Switching frequency [b]	*fs*	*Io1=IO2=5.79A*	4,5,6	400	450	600	kHz
8	effi cien cy	*η*	*Vin=28V, Io1=IO2=5.79A*	1	84	86	—	%
				2,3	82	84	-	
			Vin=42V, $I_{o1=IO2=5.79A}$	1	81	85	—	
				2,3	79	83	-	
9	Short-circuit power consumption	*PD*	*Vin=28V, output* short circuit	1,2,3	—	6	30	W
			Vin=42V, output short circuit		-	8	40	
10	Capacitive load [ab]	*CL1*、*CL2*	There is no effect on DC steady-state parameters	4	—	2000	2000	μF
11	Insulation resistance	*RISO*	Add 500VDC between the inputs, outputs, and between either pinout and housing	1	100	3000	—	MΩ
12	Output voltage change during load jump (peak) [bc]	*VLOR*	50% loaded→ full load or, full load → 50% load;	4	-950	400	950	mV
13	The recovery time of the output voltage at the time of load jump [bcd]	*tLOR*		4	—	0.3	1	ms
14	Output voltage change (peak) at input voltage jump	*VVOR*	Input voltage VI: 23→50V, *Io1=IO2=5.79A*	4	-950	400	950	mV

	be		Input voltage VI: 50→23V, *Io1=IO2=5.79A*					
15	The recovery time of the output voltage at the time of the input transition bde	*tVOR*		4	—	0.3	1	ms
16	Initiating Overshoot (Peak) b	*VTO*	Input voltage VI: = 0V→ 28V, 0V→ 42V, *Io1=IO2=5.79A*	4,5,6	—	0	475	mV
17	Startup delay bf	*tTR*	Input voltage *VI*: 0→28V, 0V→ 42V, *Io1=IO2=5.79A*	4,5,6	—	5	20	ms
18	Prohibit terminal open-circuit voltage	*VINH*	Forbidden end open circuit, *VI=28V*, 42V, *IO1=IO2=5.79A*	1	-	13	16	V
19	Protection power	*PW*	*IO1=IO2≥6.95A*	1	-	127	-	W
20	Input reflected ripple current (peak-to-peak).	*IRIP*	BW=10kHz~6MHz, VI=28V, 42V, *IO1=IO2=5.79A*, connected to EMI filter	1	-	100	300	mA
21	Input reflected ripple voltage (peak-to-peak).	*VRIP*	BW=10kHz～6MHz, *IO1=IO2=5.79A*, connected to EMI filter	1	-	120	500	mV
22	Load failure recovery time	*tLF*	*IO* from short circuit to 5.79A	4	—	3	300	ms
23	Cross adjustment degree	*SC*	70% load all the way, 30% to 70% load variation all the way	1,2,3	-	4	6	%
24	External synchronization frequency range	*fSYNC*	*IO1=IO2=5.79A*, 6 pins connected to TTL electrical Flat (VIH≥4.5V, VIL≤0.8V), Duty cycle 40%~60%	4,5,6	450	-	550	kHz

[a] Capacitive load can be anything from 0 to the maximum limit value without affecting DC parameters;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should be greater than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground.

table 15 LDCD/(20-50)-12-110/D1 Electrical Characteristic Meter

sequence number	characteristic	symbol	condition (Unless otherwise specified, -55° C≤TC≤125° C, VI= 28V±1V & VI=42V±1V, forbidden End open, CL1 = CL2 = 0, 6-pin synchronous input terminated to input ground).	Group A grouping	Limit values least	typical	utmost	single bit
1	Output voltage	VO1	IO1 = I_{O2} =4.58A	1,2,3	11.76	12.000	12.24	V
		VO2		1,2,3	-12.36	-12.000	-11.64	
2	Output current	IO1/IO2	VI=20V～50V	1,2,3	-	4.58	4.58	A
3	Output ripple voltage (Peak-Peak).	VR1	BW=10KH～6MHz, IO1 = I_{O2} =4.58A	1,2,3	-	70	150	mV
		VR2						
4	Voltage regulation	SV1	VI=20V→50V, IO1= IO2 =4.58A	1,2,3	-	10	50	mV
		SV2		1,2,3	-	10	100	
5	Load regulation	SI1	IO1 = I_{O2} =0.2A→4.58A	1,2,3	-	10	50	mV
		SI2			-	10	200	
6	Input current	IIN	Fully loaded, the preamp disables the end to connect to the input Ground	1,2,3	-	7.5	10	mA
			When fully loaded, the rear stage inhibition terminal is connected to the output ground terminal		-	70	100	
			No load, no end open road		-	65	160	
7	Enter the ripple current	IRIP	fully loaded	1	-	140	200	mA
8	Switching frequency b	fs	IO1= IO2 =4.58A	4,5,6	400	450	600	kHz
9	efficiency	η	Vin =28V, IO1= IO2 =4.58A	1	83	84.7	-	%
				2,3	81	82.5	-	
			Vin =42V, IO1 = I_{O2} =4.58A	1	82	84.5	-	
				2,3	80	82.0	-	
10	Short-circuit power consumption	PD	Vin=28V, output short circuit	1,2,3	-	21	30	W
			Vin = 42V, output short circuit	1,2,3	-	24	32	

11	Capacitive load [ab]	CL1/CL2	There is no effect on DC steady-state parameters	4	-	1000	1000	μF
12	Insulation resistance	RISO	Between inputs, outputs, and either citation Add 500VDC between the outlet and the housing	1	100	30000	-	MΩ
13	Output when the load jumps Voltage change [bc] (peak).	VLOR	50% loaded→ full load or, full load → 50%. Carry;	4	-900	600	900	mV
14	The recovery time of the output voltage at the time of load jump [bcd]	tLOR		4	-	400	900	μs
15	Input voltage is lost when it jumps Output voltage change be (peak)	VVOR	Input voltage VI: 20→50V, IO1 = I_{02} =4.58A Input voltage VI: 50→20V, IO1 = $_{IO2}$ = 4.58A	4	-1200	900	1200	mV
16	The recovery time of the output voltage at the time of the input transition [bde]	tVOR		4	-	300	900	μs
17	Start Overshoot B (Peak)	VTO	Input voltage VI: =0V→28V, IO1 = $_{IO2}$ =4.58A	4,5,6	-	0	600	mV
			Input voltage VI=0V→42V, IO1= IO2=4.58A	4,5,6	-	0	600	
18	Startup delay [f]	tTR	Input voltage VI: 0→28V, IO1 = IO2 = 4.58A	4,5,6	-	6	10	ms
			Input voltage VI: =0V→42V, IO1 = $_{IO2}$ =4.58A	4,5,6	-	6	10	
19	Prohibit terminal open-circuit voltage	VINH	Forbidden end open circuit, VI=28V, 42V, IO1=IO2=4.58A	1	-	13	16	V
20	Protection power	PW	IO1=IO2≥5.26A	1	126	126	-	W
21	When the load is recovered BD	tLF	IO from short circuit to 4.58A	4	-	6	10	ms
22	Cross adjustment degree	SC	70% load all the way, 30% all the way 70% load variation	1,2,3	-	3	6	%
23	External synchronization frequency range	fSYNC	IO1=IO2=4.58A, 6 pins TTL Level (VIH≥ 4.5V, VIL≤0.8V), duty cycle 40%~ 60%.	4,5,6	450	-	550	kHz

[a] Capacitive load can be anything from 0 to the maximum limit value without affecting DC parameters;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should be greater than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground.

table 16 LDCD/(20-50)-15-120/D1 Electrical Characteristic Meter

serial number	characteristic	symbol	condition (Unless otherwise specified, -55° C≤TC≤125° C, VI=28V±1V and VI=42V±1V, forbidden End open, CL1 = CL2 = 0, 6-pin synchronous input terminated to input ground).	Group A is grouped	Limit values			unit
					least	typical	utmost	
1	Output voltage	VO1	IO1= IO2 =4.0A	1,2,3	14.70	15.000	15.30	V
		VO2		1,2,3	-15.45	-15.000	-14.55	
2	Output current	IO1/IO2	VI=20V～50V	1,2,3	-	4.0	4.0	A
3	Output ripple voltage (Peak-Peak).	VR1	BW=10kH～6MHz, IO1 = I_{O2} =4.0A	1,2,3	-	80	150	mV
		VR2						
4	Voltage regulation	SV1	VI=20V→50V, IO1= IO2 =4.0A	1,2,3	-	10	50	mV
		SV2		1,2,3	-	10	100	
5	Load regulation	SI1	IO1= IO2 =0.2A→4.0A	1,2,3	-	10	50	mV
		SI2			-	10	200	
6	Input current	IIN	Fully loaded, the preamp disables the end to connect to the input Ground	1,2,3	-	7.5	10	mA
			When fully loaded, the rear stage inhibition terminal is connected to the output ground terminal		-	70	100	
			No load, no end open road		-	65	150	
7	Enter the ripple current	IRIP	fully loaded	1	-	140	200	mA
8	Switching frequency [b]	fs	IO1= IO2 =4.0A	4,5,6	400	450	600	kHz
9	efficiency	η	Vin =28V, IO1= IO2 =4.0A	1	84	85.5	-	%
				2,3	82	83.0	-	

			Vin =42V, IO1= IO2 =4.0A	1	83	85.0	-	
				2,3	81	73.0	-	
10	Short-circuit power consumption	PD	Vin=28V, output short circuit	1,2,3	-	21	30	W
			Vin = 42V, output short circuit	1,2,3	-	24	32	
11	Capacitive load [ab]	CL1/CL2	There is no effect on DC steady-state parameters	4	-	1000	1000	μF
12	Insulation resistance	RISO	Between inputs, outputs, and either citation Add 500VDC between the outlet and the housing	1	100	30000	-	MΩ
13	Output when the load jumps Voltage change [bc] (peak).	VLOR	50% loaded→ fully loaded or, fully loaded →50% load;	4	-900	600	900	mV
14	The recovery time of the output voltage at the time of load jump [bcd]	tLOR		4	-	400	900	μs
15	Input voltage is lost when it jumps Output voltage change be (peak)	VVOR	Input voltage VI: 20→50V, IO1= IO2 =4.0A Input voltage VI: 50→20V, IO1 = IO2 = 4.0A	4	-1500	800	1500	mV
16	The recovery time of the output voltage at the time of the input transition [bde]	tVOR		4	-	400	900	μs
17	Start the overshoot (b-peak).	VTO	Input voltage VI: =0V→28V, IO1= IO2 =4.0A	4,5,6	-	0	600	mV
			Input voltage VI: =0V→42V, IO1= IO2 =4.0A	4,5,6	-	0	600	
18	Startup delay [f]	tTR	Input voltage VI: 0→28V, IO1= IO2 =4.0A	4,5,6	-	6	10	ms
			Input voltage VI: =0V→42V, IO1= IO2 =4.0A	4,5,6	-	6	10	
19	Prohibit terminal open-circuit voltage	VINH	Forbidden end open circuit, VI=28V, 42V, IO1=IO2=4.0A	1	-	13	16	V
20	Protection power	PW	IO1=IO2≥4.6A	1	138	138	-	W
21	When the load is recovered B.D	tLF	IO from short circuit to 4.0A	4	-	6	10	ms

22	Cross adjustment degree	SC	70% load all the way, 30% all the way 70% load variation	1,2,3	-	3	6	%
23	External synchronization frequency range	fSYNC	IO1=IO2=4.0A, 6 pins connected to TTL electrical Flat (VIH≥4.5V, VIL≤0.8V), duty cycle 40%~60%.	4,5,6	450	-	550	kHz

[a] Capacitive load can be anything from 0 to the maximum limit value without affecting DC parameters;
[b] This parameter is guaranteed by design and is only tested for qualification inspection and design or process changes;
[c] The transition time of the load should be greater than 10μs;
[d] Recovery time is the time from the start of the transition until the output voltage returns to within ±1% of the corresponding stable value;
[e] The transition time of the input voltage should be greater than 200μs;
[f] The start-up delay time can be calculated either from the jump of the power supply or from the disconnection of the forbidden end of the ground.

7 Application note:

7.1 Typical Applications

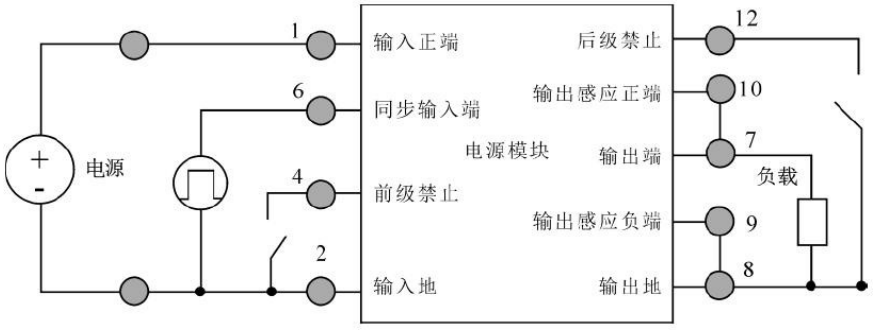


Figure 3(a) Typical application (single-channel).

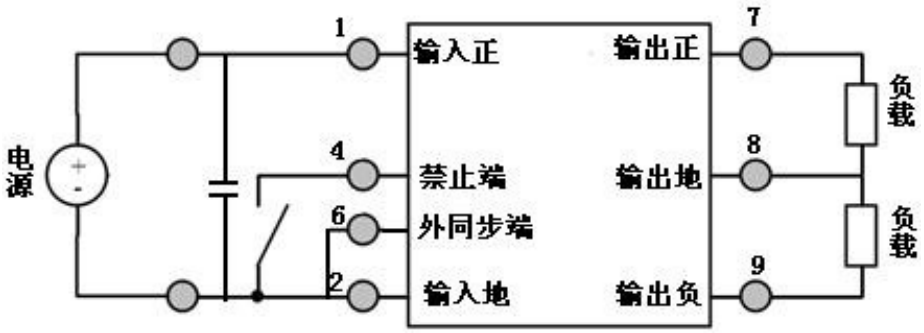


Figure 3(b) Typical application (dual).

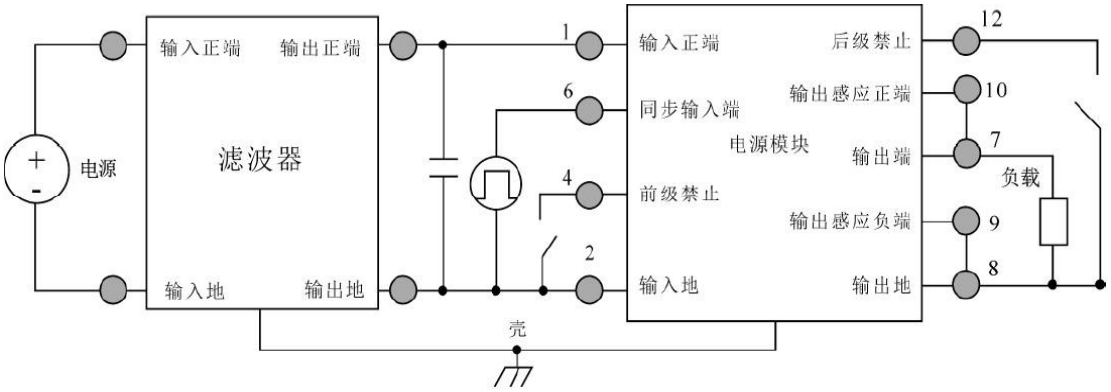


Figure 4(a) Diagram of product connection to EMI filter (single channel).

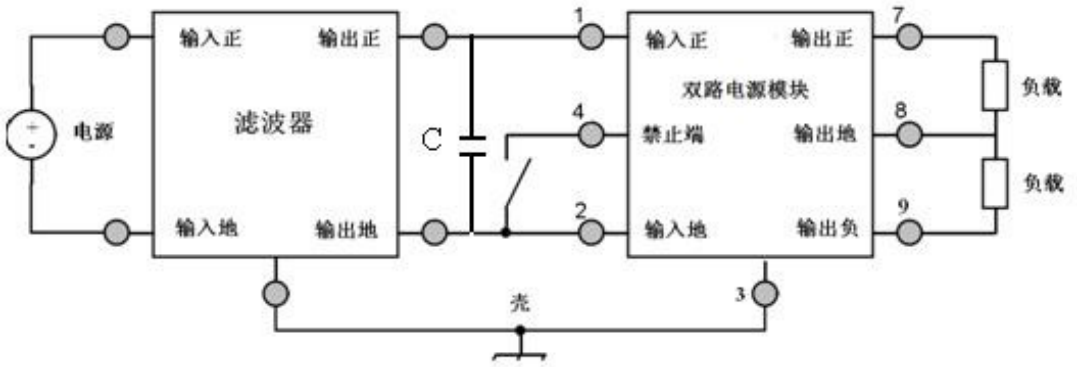


Figure 4(b) Diagram of the connection between the product and the EMI filter (dual).

7.2 Derating use

The rated output power of a DC/DC converter refers to the maximum output power that can be operated for a long time if the circuit usage conditions are met. It is generally recommended that the actual power used should not exceed 80% of the rated output power of the circuit.

Due to the difficulty of freewheeling when the load is too light, the current discontinuity will occur, resulting in unstable output voltage and no reliability problems. Generally, DC/DC converters have a minimum load limit, which is usually around 5% of the rated load. If the user has a light load or even no load use, and can not accept the increase of output ripple under the condition of no load or light load, the more convenient and effective way is to add a certain false load, about 5% of the rated load, and the user can install an appropriate resistor as the load outside the DC/DC converter.

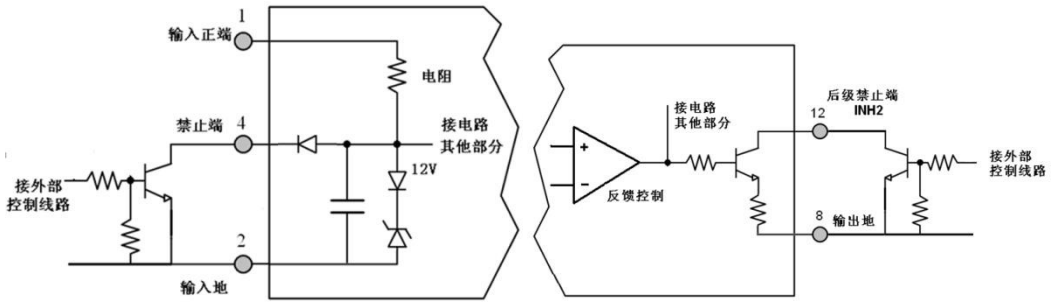
7.3 Prohibited features

The product has a pre/post-inhibition function, and the function of the inhibition terminal (INH1 or INH2) is to control whether the output voltage is present at the output terminal when the DC/DC converter is added with a specified input voltage. The forbidden side (INH1 or INH2) is used as follows:

a) When the inaway terminal (INH1 or INH2) is open, the circuit outputs normally;

b) When the inhibition terminal is enabled, the inhibition terminal (INH1 or INH2) is connected to the specified inhibition level (inhibition level≤0.8V), and the circuit has no output.

This function can be used either by connecting the inhibition port (INH) directly to ground, or by connecting an external NPN triode (base set high), as shown in Figure 5, to make the converter have no output. At the same time, when the product is designed, when the forbidden port is suspended, the pre-stage forbidden end has a DC voltage of 10V~13V, and the rear forbidden terminal has a DC voltage of 6V~10V. The resistance and capacitance parameters in the figure are designed according to the input level. If you do not use this function, you can leave it in the air.



Connection diagram of the pre-forbidden end (INH1) and the forbidden end of the posterior stage (INH2).

Figure 5 Forbidden End Connection Diagram

7.4 Input under-voltage protection function

The product has input under-voltage protection function. When the input voltage is lower than the undervoltage protection lockout threshold voltage, the product has no output power voltage.

Table 17 Input Undervoltage Protection Threshold Voltage

Product Classification	Undervoltage protection locks out the threshold voltage VOL (shutdown).	Undervoltage protection locks out the threshold voltage VOL (on).
Single-way	16V～18V	17V～19V
Two-way	16V～18V	17V～19V

7.5 The output is used at the sensing end

The circuit SENSE+ is shorted to the positive output terminal, and the SENSE- terminal is shorted to the output ground, and the circuit output is the specified output voltage.

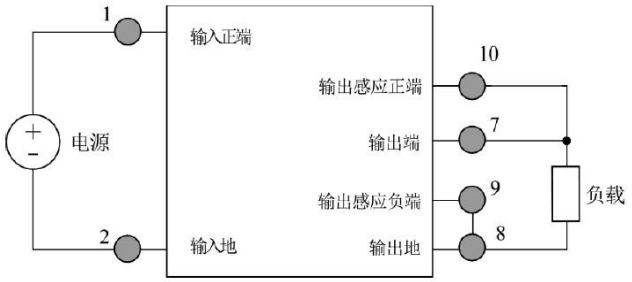


Figure 6 Connection diagram of the sensing end

7.6 The output adjustment end is used

This series of single-channel products has the function of output adjustability, and the circuit output is the specified output voltage when the output voltage adjustment terminal of the circuit is suspended. When the output voltage needs to be adjusted, the output voltage can be increased by connecting the resistor R-TRIM between the voltage regulation terminal and the output ground. The output voltage can be adjusted down by connecting the resistor R-TRIM to the positive output terminal at the voltage adjustment terminal. When the output voltage is increased and used, the maximum output current must be appropriately reduced so that the output power does not exceed the maximum output power.

When the output voltage needs to be increased, the external resistor R-TRIM is connected to the output ground, as shown in Figure 7(a), and the external resistor R-TRIM is calculated as follows:

LDCD/(20-50)-3R3-66/SP：R-TRIM=2.64/(Vo-3.3)-1

LDCD/(20-50)-5-100/SP：R-TRIM=6.25/(Vo-5)-2

LDCD/(20-50)-6R3-100/SP：R-TRIM=9.5/(Vo-6.3)-1

LDCD/(20-50)-28-112/SP：R-TRIM=(651.75-21V)/(V-28)

where Vo is the required output voltage in V; R-TRIM is an external resistor in kΩ.

When the output voltage needs to be turned down, the external resistor R-TRIM is connected to the output positive, as shown in Figure 7(b). External resistor R-TRIM calculated as follows:

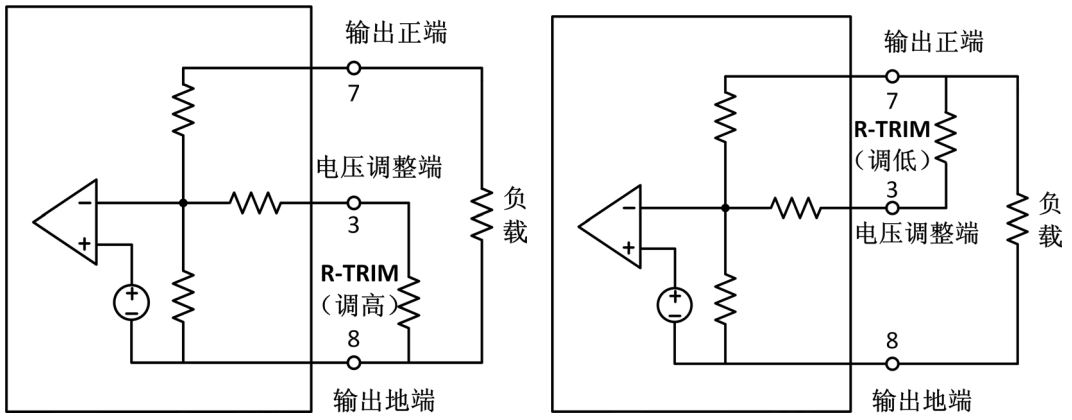
LDCD/(20-50)-3R3-66/SP：R-TRIM=0.8*(Vo-2.5)/(3.3-Vo)-1

LDCD/(20-50)-5-100/SP：R-TRIM=2.5*(Vo-2.5)/(5-Vo)-2

LDCD/(20-50)-6R3-100/SP：R-TRIM=3.8*(Vo-2.5)/(6.3-Vo)-1

LDCD/(20-50)-28-112/SP：R-TRIM=(651.75-46.5V)/(V-28)

where Vo is the required output voltage in V; R-TRIM is an external resistor in kΩ.



(a) The output is turned up by an external resistor (b) The output is turned down by the external resistor

Figure 7 R-TRIM connection

When using the TRIM function, it is easy to receive interference signals from the outside world, and if necessary, the TRIM terminal can be connected to the nearest output ground terminal (100pF~0.1μF capacitance).

Note: The output voltage regulation does not exceed ±10% of the rated voltage.

7.7 The output is used with an unbalanced load

In this series of products, the positive output of the dual-output DC/DC converter is controlled, and the negative output is transformer-coupled rectification filtering, and the output load is required to be symmetrically balanced.

7.8 Synchronization function

The product has a synchronization function, and the function of the synchronous input (SYNC) is that when multiple DC/DC converter modules are used at the same time or the system has synchronous frequency requirements, it can be used to control the internal switching frequency of multiple DC/DC converter modules to operate at the same frequency, or to make DC/DC The switching frequency inside the converter module matches the system clock frequency.

The Sync Input (SYNC) is used as follows:

a) When the synchronization function is used, the synchronization input termination is as follows: frequency range 450kHz~500kHz, duty cycle 40%~60%, TTL level, low level≤ 0.8V, 4.5V≤ high level≤5.0V.

b) When the synchronization function is not in use, it is recommended that the synchronization input terminate the input ground. If the synchronous output is not in use, consult the supplier when using it.

c) When using the synchronous input function, the DC/DC converter output load is required to be ≥ 20%.

7.9 Current sharing function

When using the current sharing function, the user should ensure that the impedance between the output and the load of each circuit is consistent, and pay attention to the bias current problem, especially when the load is dynamic.

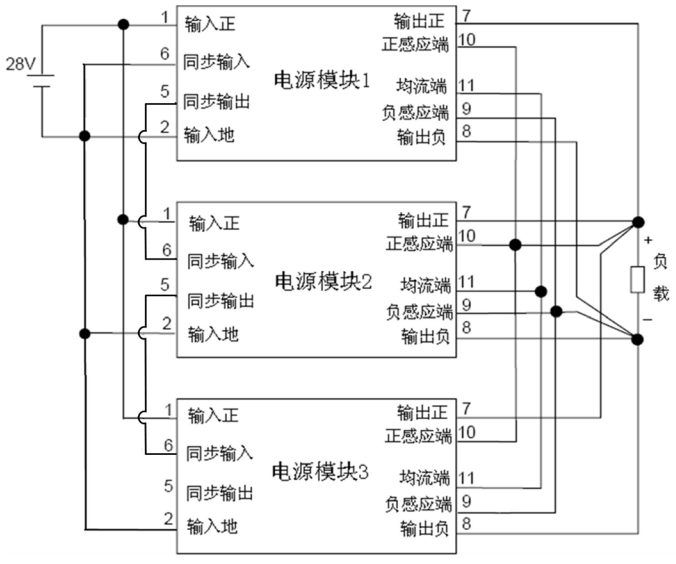


Figure 8 Diagram of the connection of the current sharing function

When using the current sharing function, the output power of each power module is recommended to be within the range of 20%-80% of the rated load; The operating frequency of each power module needs to be consistent. Signals can be used to synchronize each power module; It can also be cascaded, the synchronous output of the first power module is connected to the synchronous input of the second power module, and the synchronous output of the second power module is connected Synchronous input of three power modules, up to three power modules for current sharing.

Table 18 Current sharing accuracy of LDCD/(20-50)-5-100/SP two power modules in parallel

Total output current (A).	Module 1 output current (A).	Module 2 output current (A).
10	3.9	6.1
12	4.9	7.1
14	5.9	8.1
16	7.3	8.7
18	8.7	9.3
20	9.8	10.2
22	10.9	11.1
24	11.9	12.1
26	12.9	13.1
28	13.9	14.1
30	14.9	15.1
32	16.0	16.0

Table 19 Current sharing accuracy of LDCD/(20-50)-6R3-100/SP two power modules in parallel

Total output current (A).	Module 1 output current (A).	Module 2 output current (A).
8	4.2	3.8
10	5.3	4.8
12	6.2	5.8
14	7.2	6.8
16	8.1	7.9
18	9.1	8.9
20	10.1	9.9
22	11.1	10.9
24	12.1	11.9
26	13.0	13.0

Table 20 Current sharing accuracy of LDCD/(20-50)-28-112/SP two power modules in parallel

Total output current (A).	Module 1 output current (A).	Module 2 output current (A).
1	0.8	0.2
2	1.2	0.8
3	1.7	1.3
4	2.1	1.9
5	2.6	2.4
6	3.0	3.0
7	3.6	3.4

7.9 Capacitive load use

Within the capacitive load range specified in the detailed specification, the capacitive load capacity does not decrease with the change of input voltage, output load, temperature, and consult the supplier when the user's capacitive load exceeds the maximum specified in the procurement specification.

7.10 Front-end surge circuit design

The device has an LC filter line on the internal input, and inrush current is unavoidable at the moment the power supply is started, so it is recommended that users use this product to add a surge suppression line or use an EMI filter with a built-in surge suppression line .

A schematic diagram of the recommended surge suppression circuit is shown in Figure 9

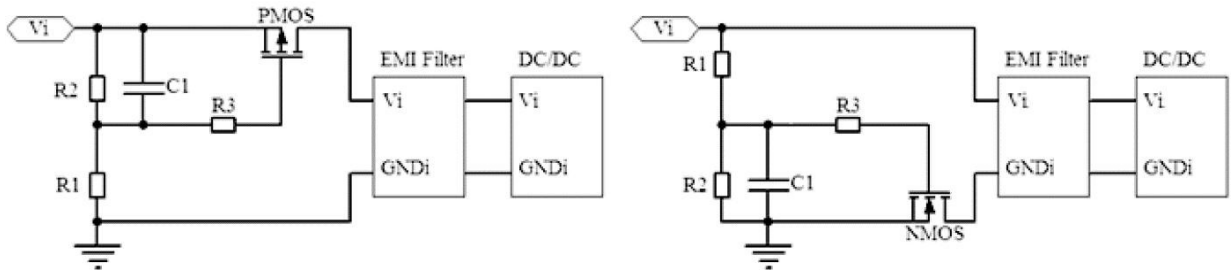
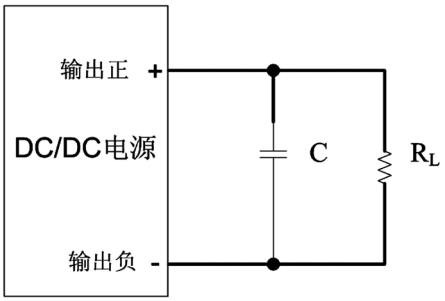


Figure 9 Schematic diagram of the surge suppression line

The withstand voltage of the P-channel, N-channel MOSFETs should be greater than 100V. The inrush current suppression is related to the peripheral resistance and capacitance parameters, and the size of resistors R1, R2, R3, and capacitance C1 is adjusted by the user according to the actual application of the system.

7.11 Output filter circuit design

LC filtering circuitry is used in the internal design of the device. If the output ripple of the product does not meet the system requirements, the user can filter the output of the DC/DC converter to reduce the ripple. The schematic diagram is as follows:



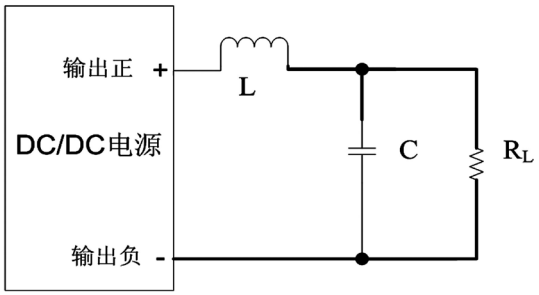


fig 10 Schematic diagram of capacitors fig 11 pick up LC Schematic diagram of filtering

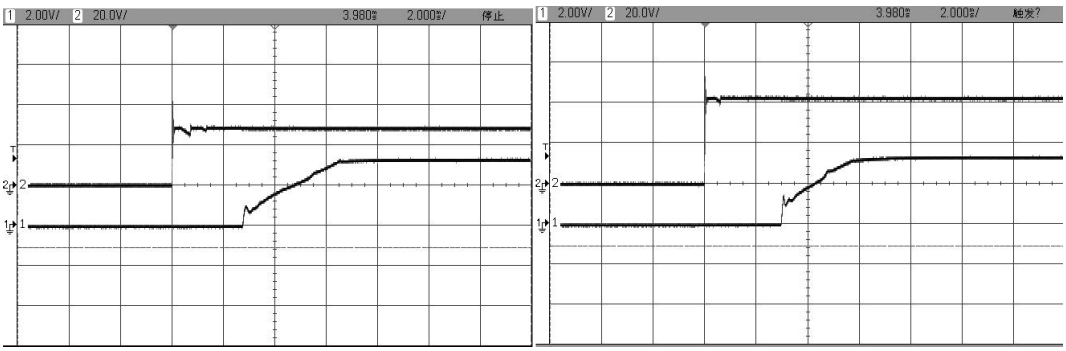
The capacitor should be as close to the load as possible, and the capacitance of the external capacitor should be less than the capacity of the DC/DC converter to carry capacitive loads; The inductance of the inductor L is adjusted according to the actual situation.

8 Radiation resistance

The product adopts single-ended forward and magnetically isolated feedback topology, and the internal core chip selects self-developed irradiation reinforcement devices. Resistance to total dose irradiation up to 100krad(Si) at a dose rate of 0.1rad(Si)/s; The anti-single particle threshold LET is 75MeV·cm^2/mg.

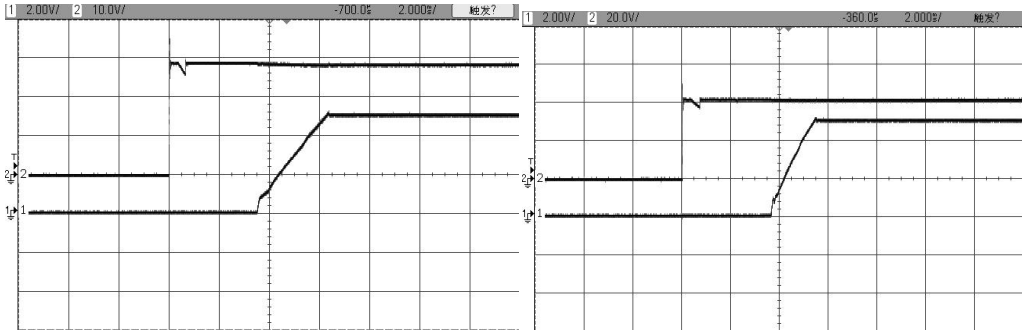
9 Product performance waveform

9.1 Start-up delay/start-up overshoot (Tc=25° C, full load).



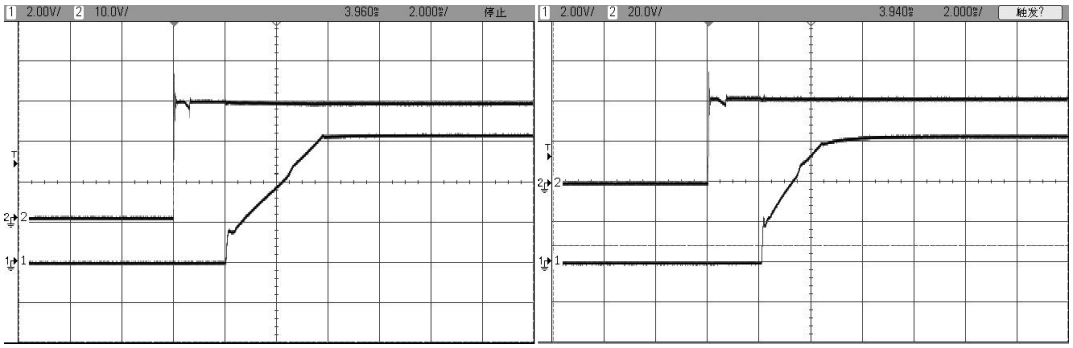
VI=28V Startup delay 6.1ms VI=42V Startup delay 5.8ms

Figure 12 LDCD/(20-50)-3R3-66/SP: Initiation overshoot/delay



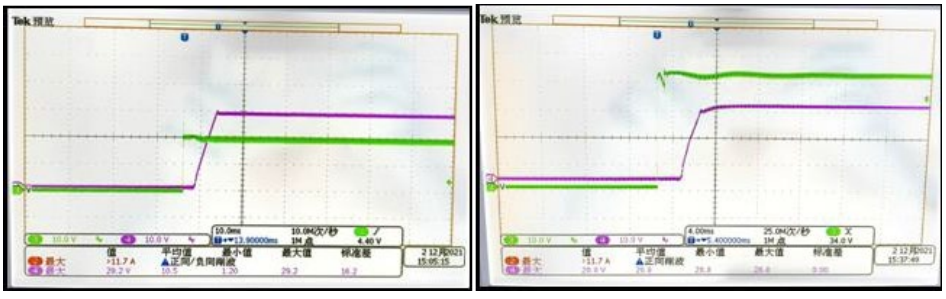
VI=28V Startup delay 6.1ms VI=42V Startup delay 5.4ms

Figure 13 LDCD/(20-50)-5-100/SP: Initiation overshoot/delay



VI=28V Startup delay 5.6ms VI=42V Startup delay 5.4ms

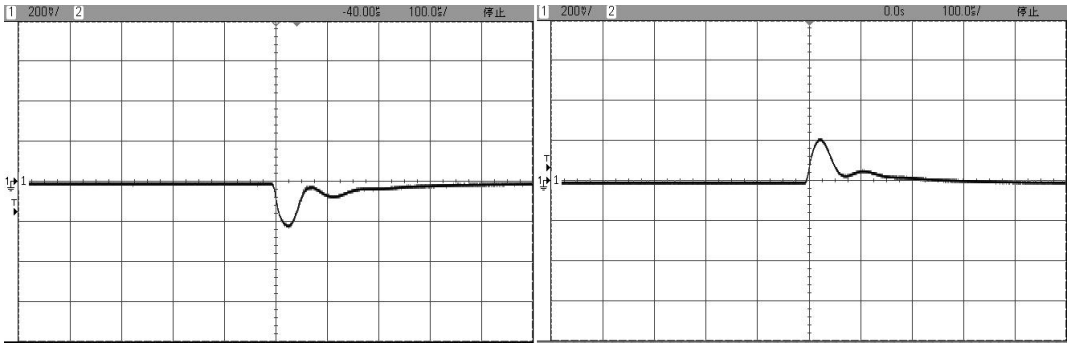
Figure 14 LDCD/(20-50)-6R3-100/SP: Initiation overshoot/delay



VI=28V Startup delay 3.5ms VI=42V Startup delay 4.8ms

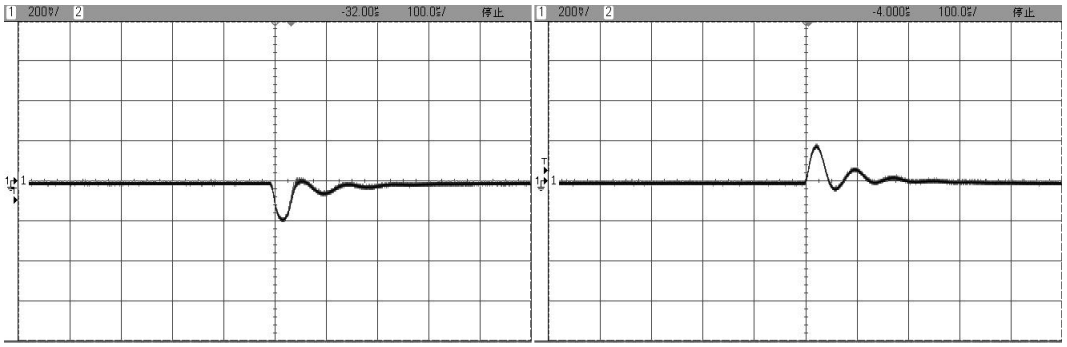
Figure 15 LDCD/(20-50)-28-112/SP: Initiation overshoot/delay

9.2 Transient waveform of output voltage (Tc = 25° C, VI = 28V± 0.5V,42V± 0.5V) when the load step changes



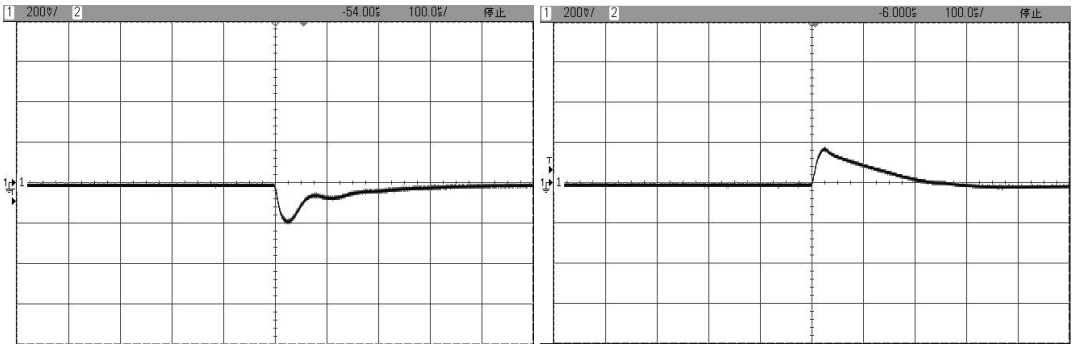
VI=28V, output 50% load→ full load variation　　VI=28V, 50% load change → full load

Figure 16(a) LDCD/(20-50)-3R3-66/SP load step 1



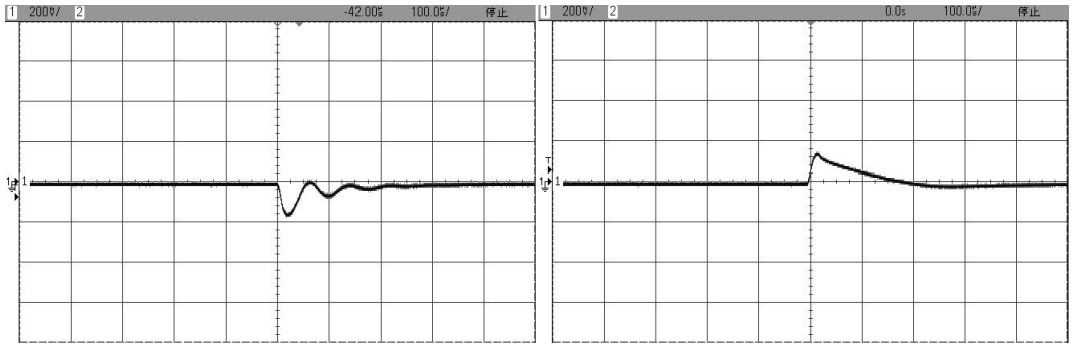
VI=42V, output 50%Load → full load variation　　VI=42V, 50% load change → full load

Figure 16(b) LDCD/(20-50)-3R3-66/SP Load steps 2



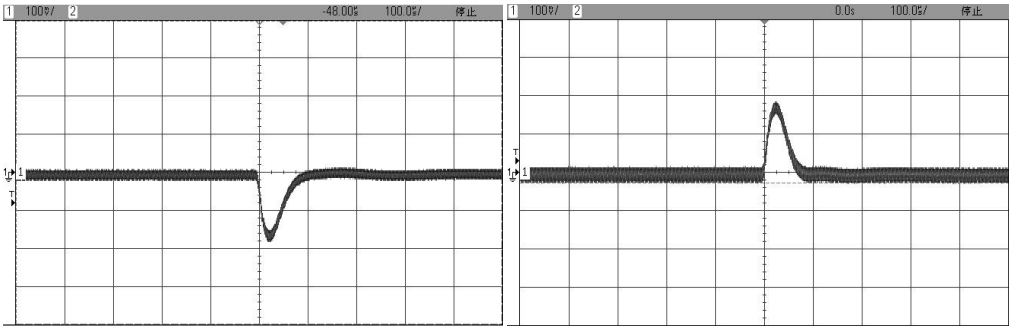
VI=28V, Output 10% load → 50% load change　　VI=28V, 50% load → 10% load variation

Figure 16(c) LDCD/(20-50)-3R3-66/SP Load steps 3



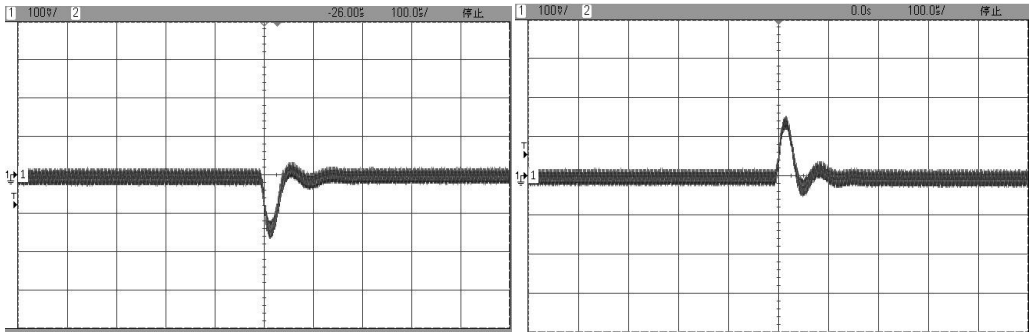
VI=42V, Output 10% load → 50% load change　　VI=42V, 50% load → 10% load variation

Figure 16(d) LDCD/(20-50)-3R3-66/SP Load steps 4



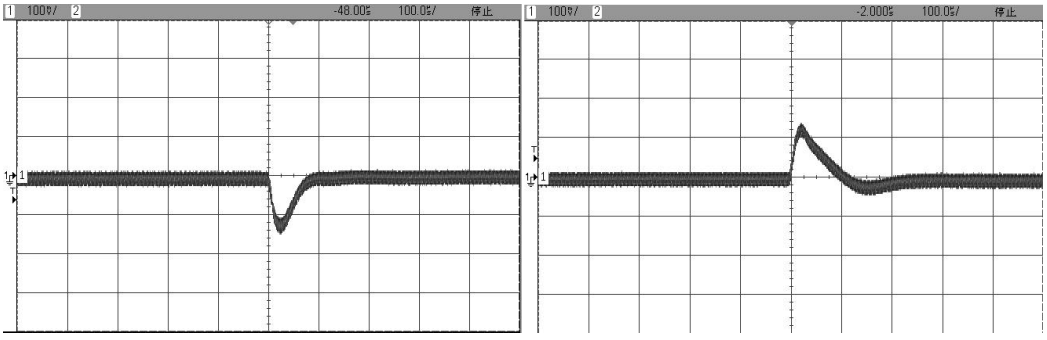
VI=28V, output 50% load→ full load variation　　VI=28V, full load→50% load variation

Figure 17(a) LDCD/(20-50)-5-100/SP load step 1

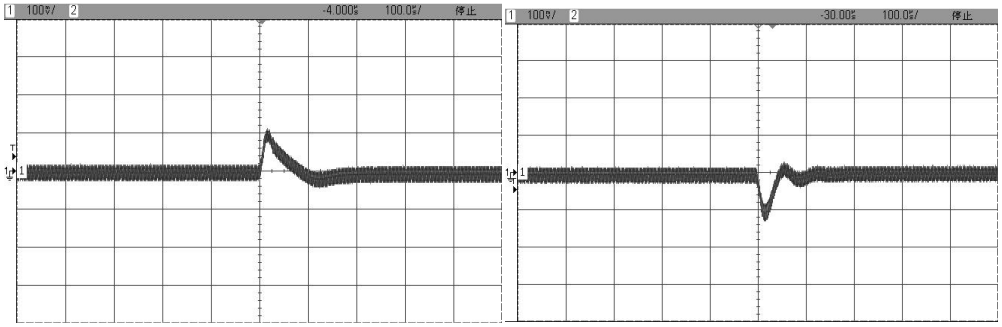


VI=42V, output 50%Load → full load variation　　VI=42V, 50% load change → full load

Figure 17(b) LDCD/(20-50)-5-100/SP Load steps 2

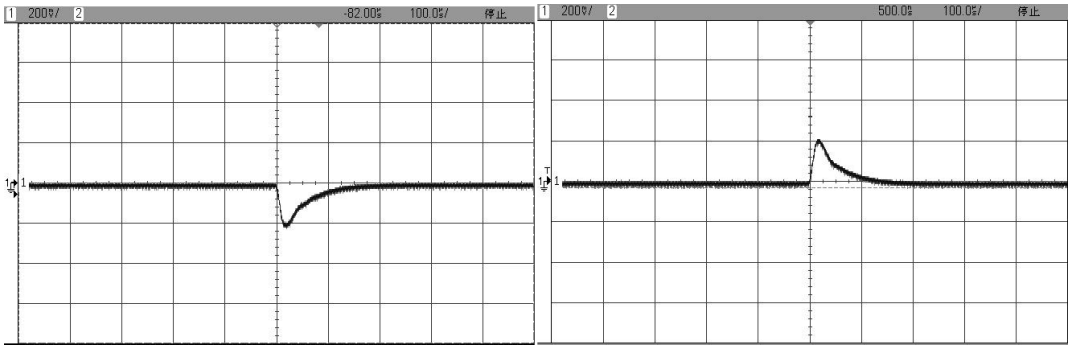


VI=28V, output 10%Load → 50% load variation　　VI=28V, 50%Load → 10% load change Figure 17(c) LDCD/(20-50)-5-100/SP Load steps 3



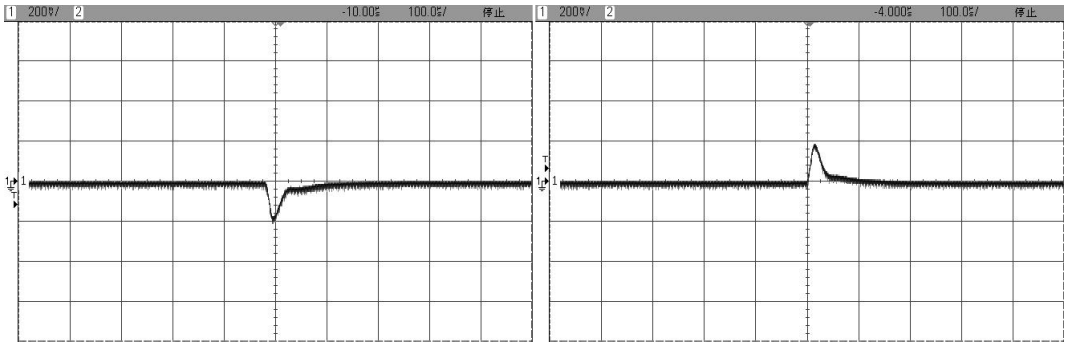
VI=42V, output 10%Load → 50% load variation VI=42V, 50%Load → 10% load change

Figure 17(d) LDCD/(20-50)-5-100/SP Load steps 4



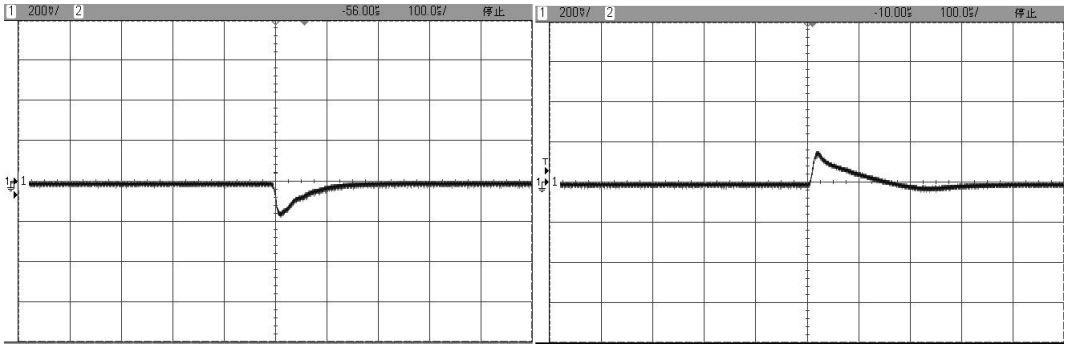
VI=28V, output 50% load→ full load variation VI=28V, full load→50% load variation

Figure 18(a) LDCD/(20-50)- 6R3-100/SP load step 1



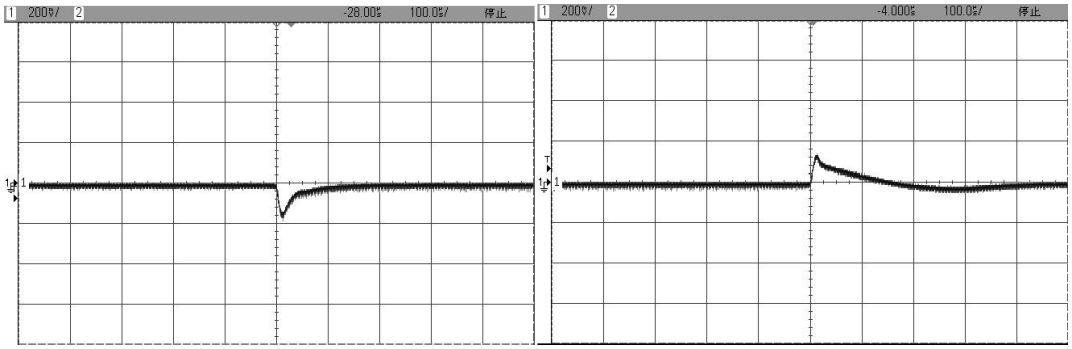
VI=42V, output 50%Load → full load variation VI=42V, full load → 50% load change

Figure 18(b) LDCD/(20-50)- 6R3-100/SP Load steps 2



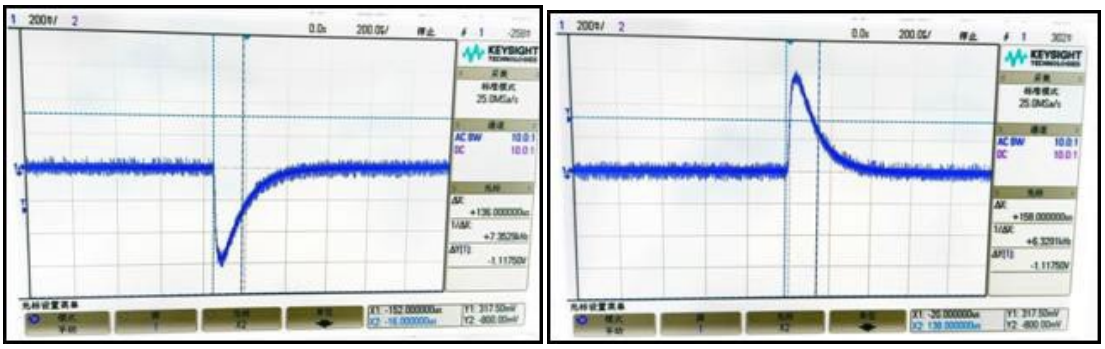
VI=28V, output 10%Load→50%Load changes VI=28V, 50%Load → 10% load change

Figure 18(c) LDCD/(20-50)- 6R3-100/SP Load steps 3



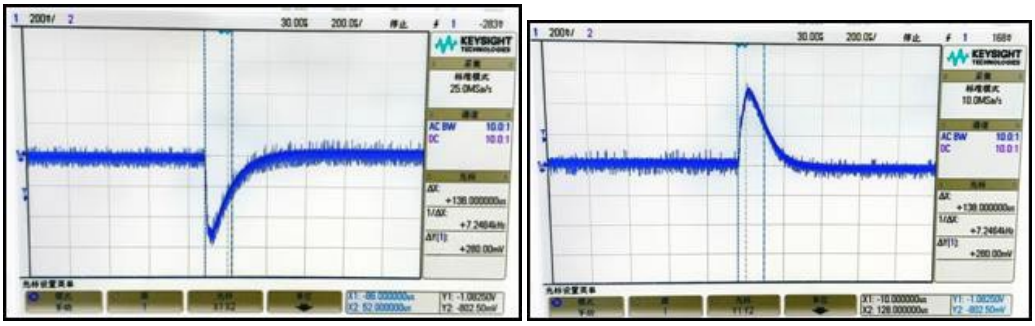
VI=42V, output 10%Load→50%Load changes　　VI=42V, 50%Load → 10% load change

Figure 18(d) LDCD/(20-50)- 6R3-100/SP Load steps 4



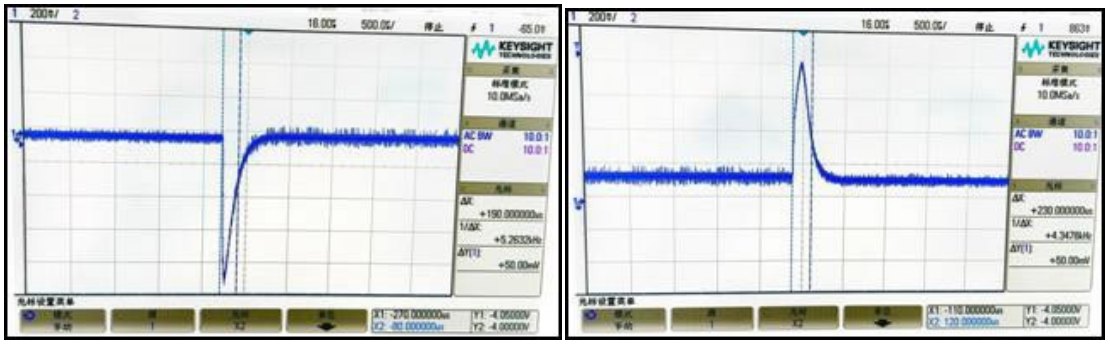
VI=28V, output 50%Load → full load variation　　VI=28V, full load → 50% load change

Figure 19(a) LDCD/(20-50)-28-112/SP Load steps 1



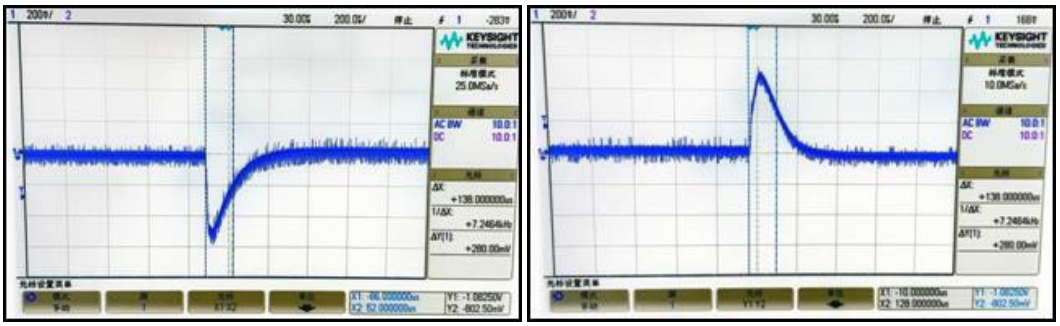
VI=42V, output 50%Load → full load variation　　VI=42V, full load → 50% load change

Figure 19(b) LDCD/(20-50)-28-112/SP Load steps 2



VI=28V, output 10%Load→50%Load changes　　VI=28V, 50%Load → 10% load change

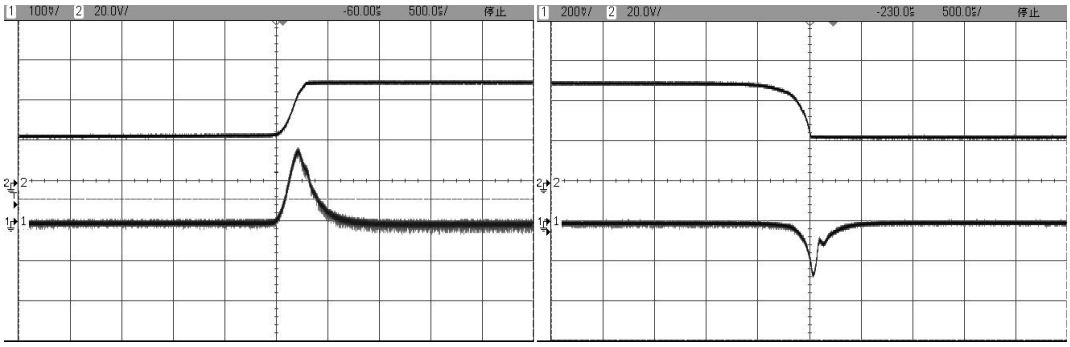
Figure 19(c) LDCD/(20-50)-28-112/SP Load steps 3



VI=42V, output 10%Load→50%Load changes　　VI=42V, 50%Load → 10% load change

Figure 19(d) LDCD/(20-50)-28-112/SP Load steps 4

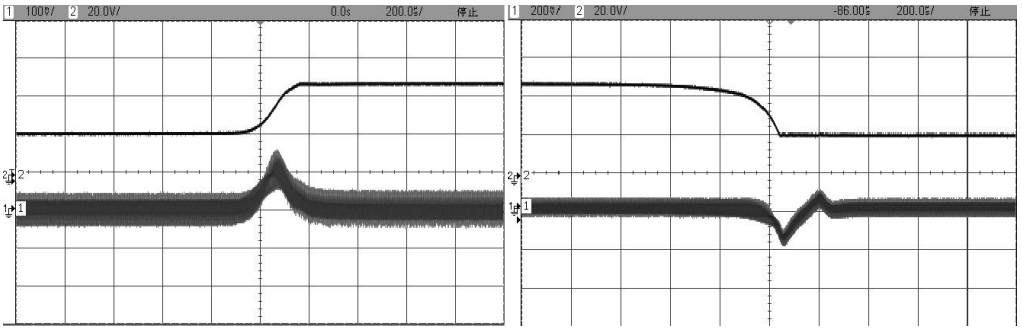
9.3 The output voltage transient waveform (Tc = 25° C, full load) when the input voltage step changes



VI: 23V→50V , the output voltage changes the waveform

VI: 50V→23V , the output voltage changes the waveform

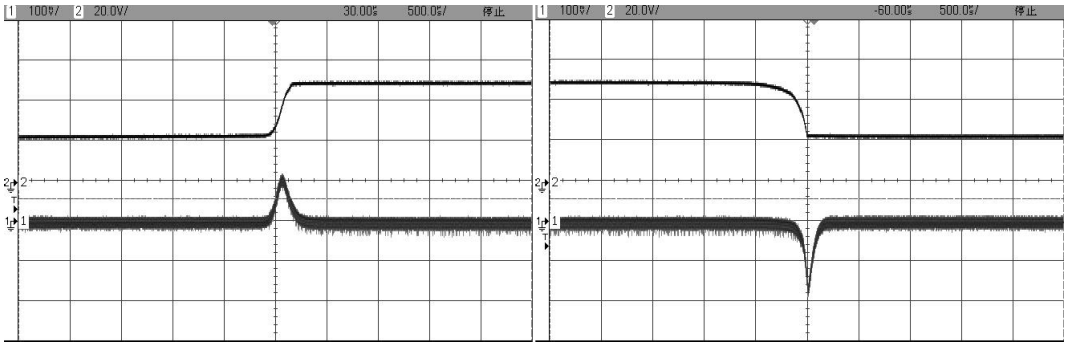
Figure 20 LDCD/(20-50)-3R3-66/SP input step



VI: 20V→50V , the output voltage changes the waveform

VI: 50V→20V , the output voltage change waveform

Figure 21 LDCD/(20-50)-5-100/SP Enter a step



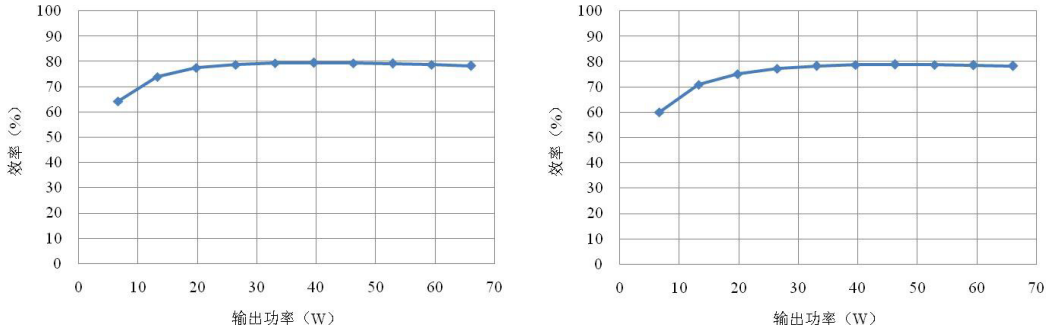
VI：23V→50V , the output voltage changes the waveform

VI：50V→23V , the output voltage change waveform

Figure 22 LDCD/(20-50)- 6R3-100/SP Enter a step

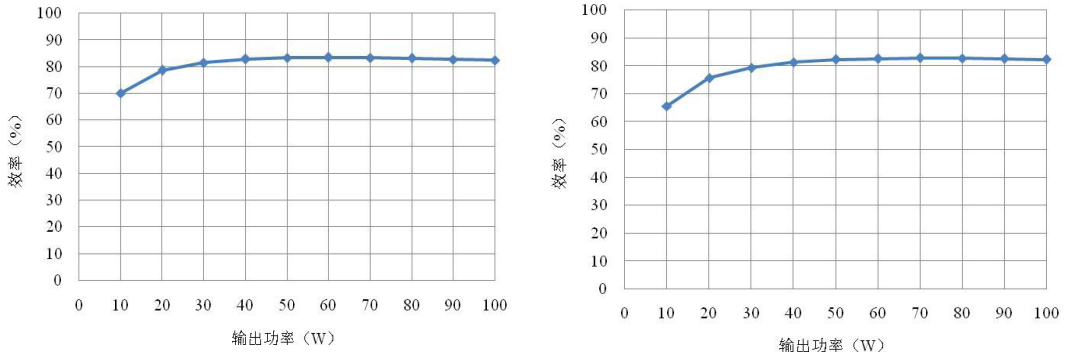
10 Efficiency characteristic curve

10.1 Efficiency varies with output power (Tc=25° C, Vin=28V, 42V).



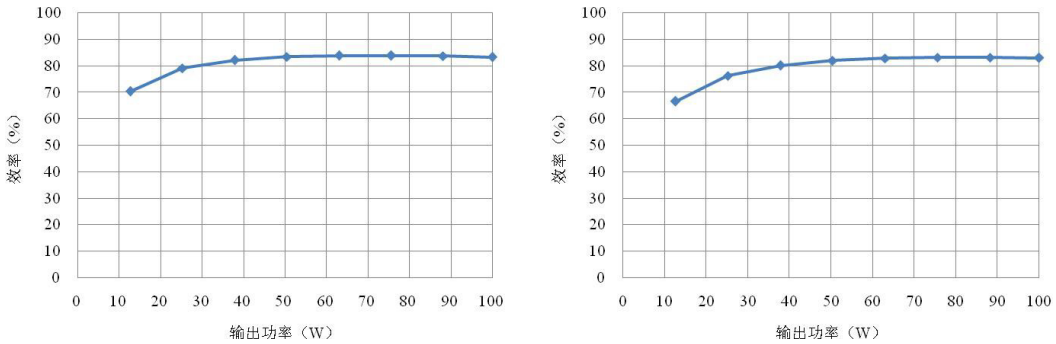
(a) Efficiency-output power curve at Vin=28V (b) Efficiency-output power curve at Vin = 42V

Figure 23LDCD/(20-50)-3R3-66/SP efficiency-output power curve



(a) Efficiency-output power curve at Vin=28V (b) Efficiency-output power curve at Vin = 42V

Figure 24 LDCD/(20-50)-5-100/SP efficiency-output power curve



(a) Efficiency-output power curve at Vin=28V (b) Efficiency-output power curve at Vin = 42V

Figure 25LDCD/(20-50)-6R3-100/SP efficiency-output power curve

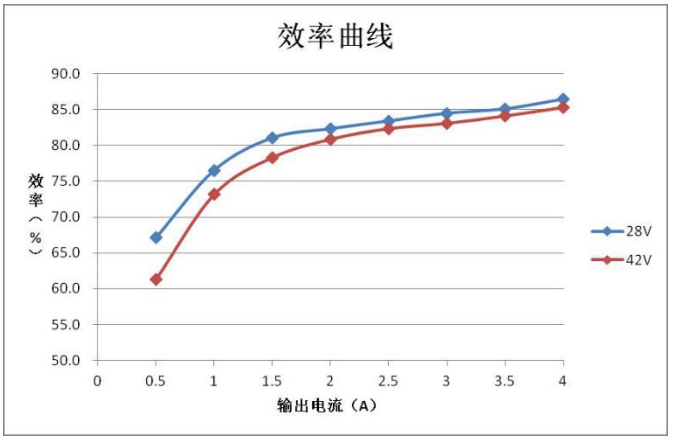


Figure 26 LDCD/(20-50)-28-112/SP efficiency-output power curve

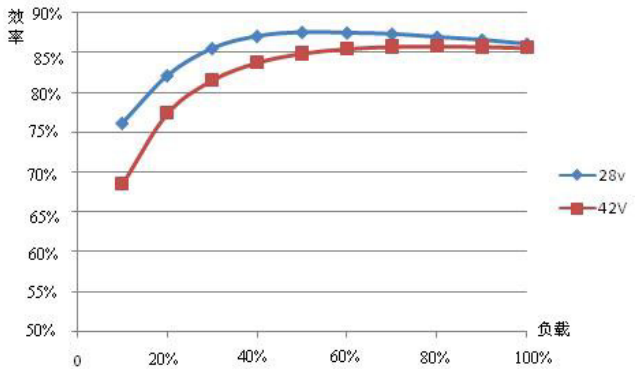


Figure 27LDCD/(20-50)-12-110/D1 efficiency-output power curve

10.2 Efficiency vs. input voltage (Tc=25° C, full load).

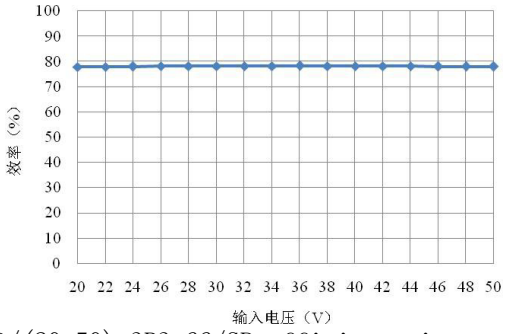


Figure 28 LDCD/(20-50)-3R3-66/SP efficiency-input voltage curve

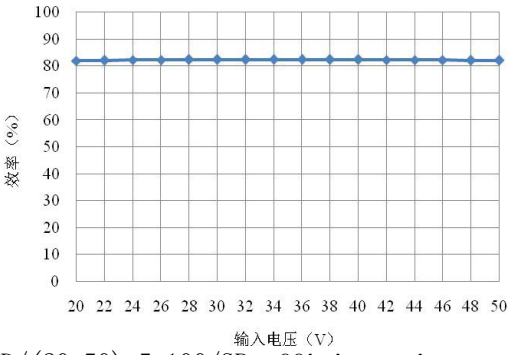


Figure 29 LDCD/(20-50)-5-100/SP efficiency-input voltage curve

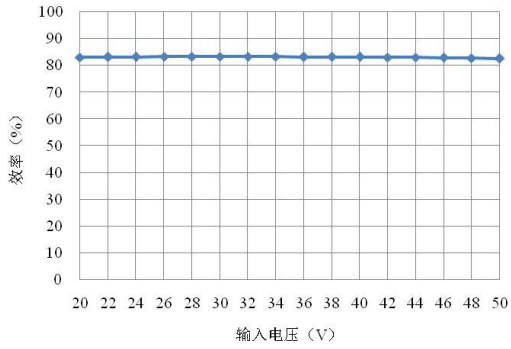


Figure 30 LDCD/(20-50)- 6R3-100/SP efficiency-input voltage curve

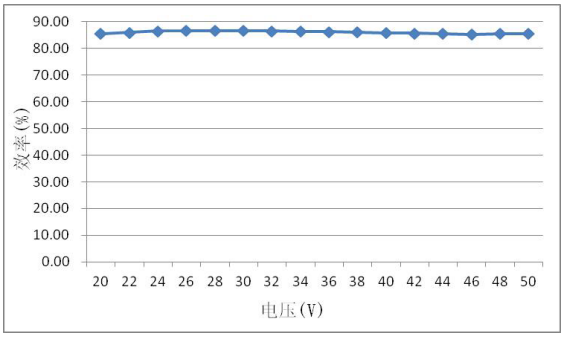


Figure 31 LDCD/(20-50)-28-112/SP efficiency-input voltage curve

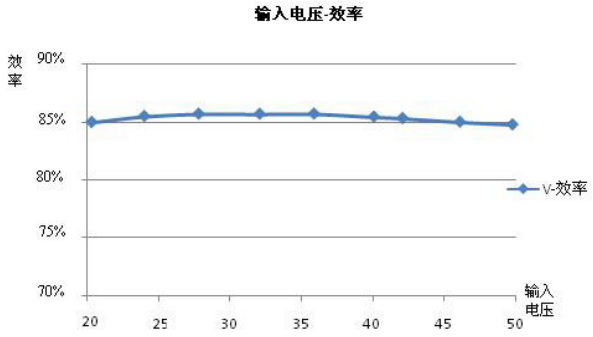


Figure 32 LDCD/(20-50)-12-110/D1 efficiency-input voltage curve

11 MTBF curve (environmental category: Aerospace Flight).

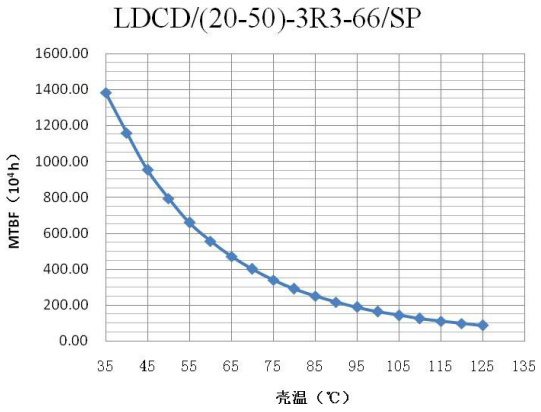


Figure 33 LDCD/(20-50)-3R3-66/SP MTBF curve

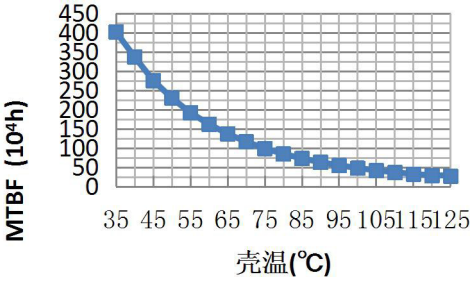


Figure 34 LDCD/(20-50)-5-100/SP MTBF curve

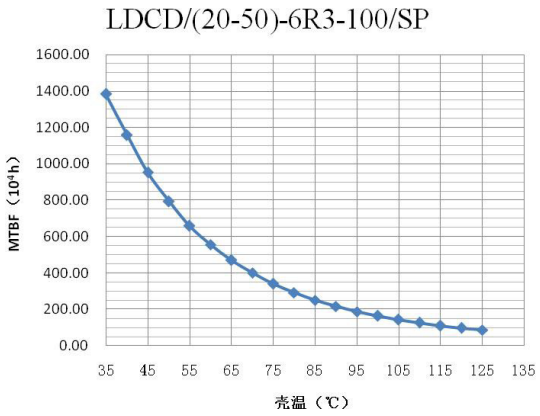


Figure 35 LDCD/(20-50)-6R3-100/SP MTBF curve

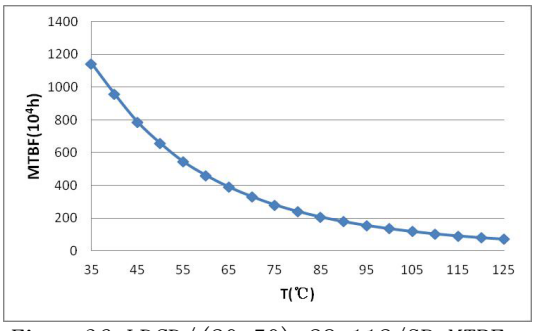


Figure 36 LDCD/(20-50)-28-112/SP MTBF curve

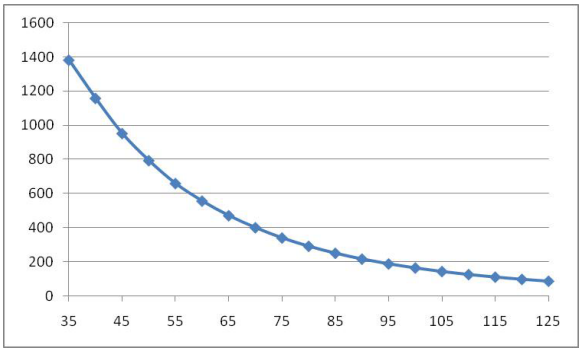


Figure 37 LDCD/(20-50)-12-110/D1 curve

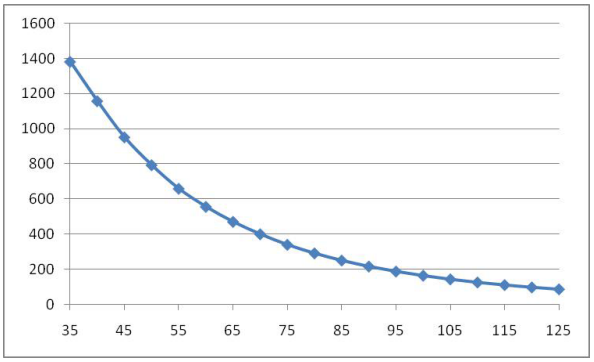


Figure 38 LDCD/(20-50)-15-120/D1 curve

The operating temperature of the DC/DC changer directly affects the life of the DC/DC changer, and the lower the operating temperature, the longer the DC/DC changer life. Under certain operating conditions, the loss of DC/DC changer is certain, and its temperature rise can be reduced by improving the heat dissipation conditions of DC/DC changer, thereby greatly extending its service life.

12 Internal thermal resistance and thermal design use

table 21 Thermal resistance value in the series

Product name	Internal thermal resistance (° C/W).	Maximum power consumption (W).	Heatsink size (mm3).	Heat sink material
LDCD/(20-50)-3R3-66/SP	0.91	18.6	174×100×3	copper
LDCD/(20-50)-5-100/SP	1.0	25	174×100×3	copper
LDCD/(20-50)-6R3-100/SP	1.10	20	174×100×3	copper
LDCD/(20-50)-28-112/SP	0.71	21	174×100×3	copper
LDCD/(20-50)-12-110/D1	1.11	22.5	174×100×3	copper
LDCD/(20-50)-15-120/D1	1.11	22.5	174×100×3	copper

The maximum operating temperature of a DC/DC converter refers to the upper temperature limit of its product housing, that is, in any case, it is ensured that the temperature of the product housing does not exceed the rated maximum operating temperature. As a product of power integration, the DC/DC converter generates more heat during operation, so in order to ensure the reliable use of the product, certain heat dissipation measures must be taken for the DC/DC

converter. Apply an appropriate heat sink according to the power consumption, and make the DC/DC converter module in good contact with the heat sink, and the heat transfer medium between the heat sink and the DC/DC converter module base plate should have good thermal conductivity, it is recommended to use a thermal pad or thermal grease, and the shell temperature of the circuit module can not exceed 125 ° C.

13 Filter items and criteria

Table 22 Filter Items and Criteria

sequence number	project	GJB 548B -2005		request		
		method	condition	Class H	YB level	Number of samples
1	Non-destructive bond pull	2023	—	Not requirement	request	10% of the sample is taken and all the internal leads are checked, and if it fails 100% conducted
2	Stability roast	1008	150℃, 24h	request	request	100%
3	Internal visual inspection	2017	—	Condition H grade	Condition Grade K	100%
4c	Temperature cycling	1010	Condition C, 10 times	request	request	100%
5c	Constant acceleration	2001	29400m/s^2, Y1 direction	request	request	100%
6	Particle Collision Noise Detection (PIND).	2020	Condition A	request	request	100%
7	Electrical test before aging	—	According to the detailed specification table 1, table 3	request	request	100%
8	Aging test	1015	TC=125° C test protocol and old trial The circuit diagram is shown in Figure 5	Time 160h	Time 240h	100%
9	Electrical test after aging test	—	According to the detailed specification table 1,	request	request	100%

				table 3			
10	Calculate the amount of change and the rate of non-conforming products		—	According to the detailed specifications Table 1, Table 2, Table 3 stipulate	Not requirement	request	100%
11	Permissible Non-Defect Rate (PDA).		—	—	request	request	5% or 1 piece (whichever is greater)
13	seal	Careful leak detection	1014	—	A1 or A2	A1	100%
		Gross leak detection		C1	request	request	100%
14	X-rays		2012	Perpendicular to the orientation of the substrate mounting	request	request	100%
15	External visual inspection		2009	—	request	request	100%

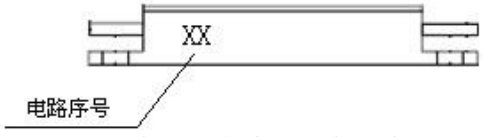
14 Logo and name

The product mark is formulated in accordance with the provisions of 3.16 and detailed specifications in Q/QJA 20085-2012, mainly including: device identification number; anchors; batch identification code or date code; the name or trademark of the contractor; Circuit product serial number; Electrostatic Discharge Susceptibility (ESDS) identification number. The device identification numbers are as follows (take LDCD/(20-50)-3R3-66/SP as an example).

YC LDCD/(20-50)-3R3-66/SP Mb C R

Quality grade Part number Housing profile Lead coating RHA sign

Among them, the quality grade: YC grade, in the upper right corner of the logo face marked as "YC"; Case Profile: Metal flat package with MB designation. "△△" is used as the identification mark of the positioning point (the first



pinout), and at the same time as the symbol of the electrostatic sensitive circuit. Each circuit should be marked with a batch identification code that identifies the seal week and a unique, consecutively given serial number.

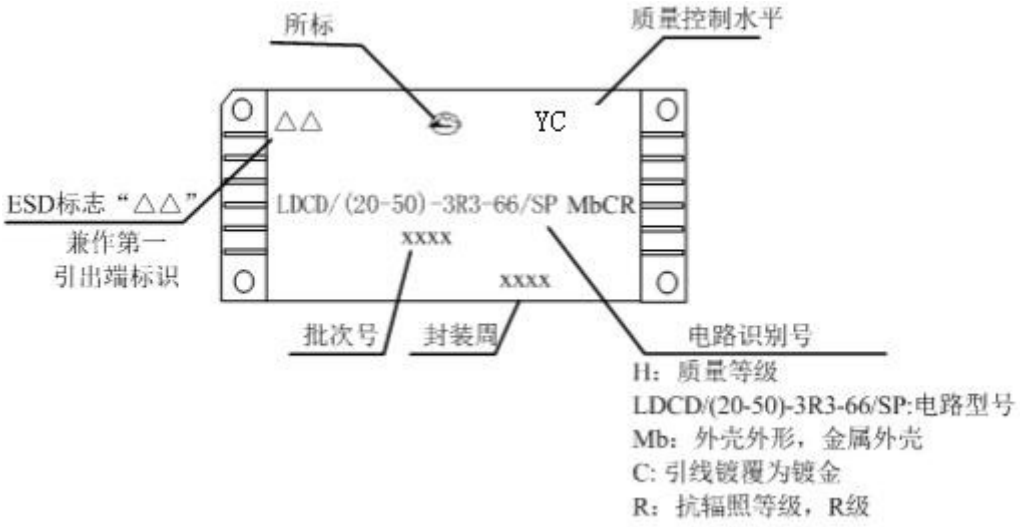


Figure 39 Schematic diagram of the product logo

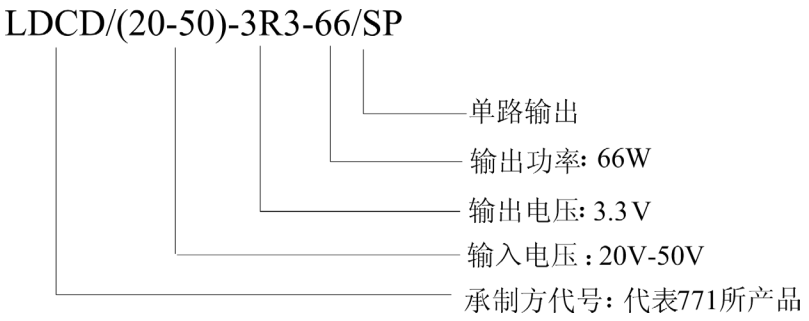


Figure 40(a) LDCD/(20-50)-3R3-66/SP, LDCD/(20-50)-5-100/SP, LDCD/(20-50)-6R3-100/SP, LDCD/(20-50)-8-100/SP、LDCD/(20-50)-9R5-110/SP、LDCD/(20-50)-12-110/SP、LDCD/(20-50)-15-120/SP、LDCD/(20-50)-20-120/SP, LDCD/(20-50)-28-112/SP product model diagram

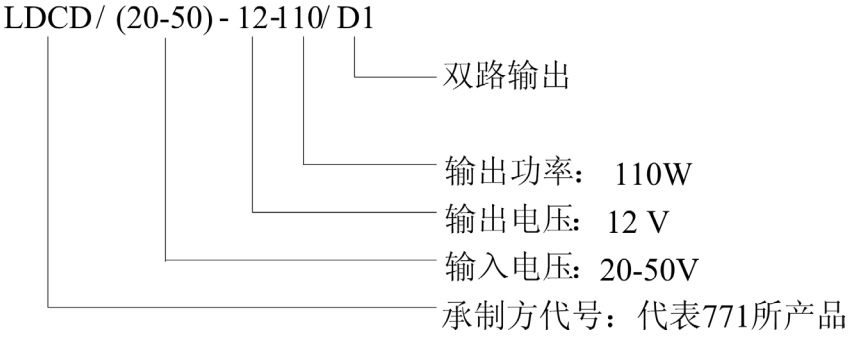


Figure 40(b) LDCD/(20-50)-5-100/D1, LDCD/(20-50)-9R5-110/D1, LDCD/(20-50)-12-110/D1, LDCD/(20-50)-15-120/D1 model diagram

15 Package outline drawing, dimensions and description

The unit is mm

Dimension symbols	numeric value		
	least	Nominal	utmost
A	9.46	-	10.66
A1a	-	5.59	-
A2	1.07	-	1.47
ϕb	0.8	-	1.2
D	75.7	-	76.70
ea	-	5.08	-
E	37.8	-	38.60
L	5.35	-	6.35
ϕP	-	3.30	-
X1a	-	70.10	-
X2	63.00	-	64.00

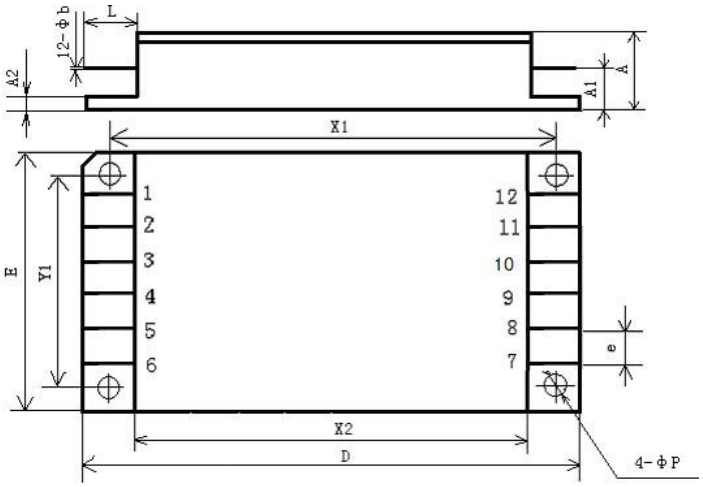


Figure 41 Exterior Dimension Drawing

16 Precautions

(1) It is forbidden to pull and bend the shell pins during transportation and use, so as not to damage the pin insulators and affect the sealing and long-term reliability of the product;

(2) The polarity of the input voltage cannot be reversed;

(3) There are polar tantalum capacitors inside the output end of the circuit of this product, and the polarity of the table pen should be tested when the impedance test of the output end is carried out;

(4) It is forbidden to plug and unplug the circuit with electricity;

(5) In the process of storage, transportation, installation and commissioning, anti-static measures should be implemented;

(6) Storage, use, and welding shall be in accordance with the provisions of Article 3 "Conditions of Use";

(7) The output should not be short-circuited for a long time to avoid the shell temperature exceeding 125° C;

(8) It is recommended that the time of the rising edge of the bus voltage >1ms;

(9) When the DC/DC module starts, there will be a start-up current requirement, and it is recommended to set the input power protection point to more than 2 times the current required for normal operation ;

(10) The DC/DC converter output protection power is limited to 1.15 times the rated output power, and if the load current (including steady-state current and start-up instantaneous current) exceeds 1.15 times, the DC/DC converter may enter an overcurrent protection state;

(11) When using one filter with multiple DC/DC converters, a mismatch between the impedance of the filter and the DC/DC converter may occur, causing the circuit to oscillate, at the output of the EMI filter and the DC/DC The differential mode capacitor is added to the input of the converter, as shown in Figure 42 below.

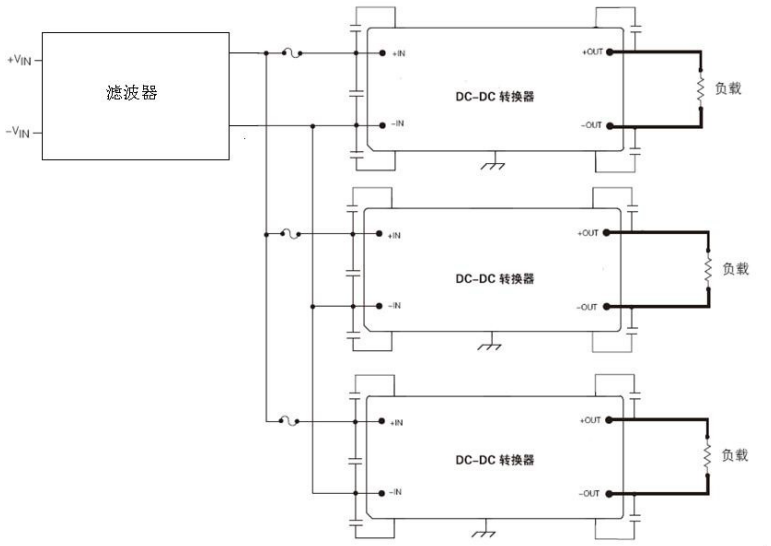


Figure 42 Typical Application Connections

(12) If multiple DC/DC converters are applied on the same printed board, common-mode noise crosstalk oscillation may occur, and a common-mode capacitor (1000pF~0.1μF) is connected to the shell at the input and output terminals of the DC/DC converter respectively, and the capacitor should meet the insulation withstand voltage requirements of the outer shell at the input and output terminals, as shown in Figure 42 below;

(13) In the process of circuit start-up, the external voltage at the output terminal may cause the circuit to start abnormally, so the output terminal is not allowed to apply voltage, in the multi-module or single-module multi-channel (three or more) output, should check whether there is a latent path between the outputs, if there is a latent path, the diode should be used for isolation;

(14) The DC/DC converter is a power device, and the bus current is large during start-up and operation, so it is not recommended to connect the resistor in series on the input bus, so as not to produce voltage drop and affect the start-up performance of the circuit;

(15) If the DC/DC converter load is a switching power supply (such as point-of-load power supply, high-frequency pulsating load, etc.), it may oscillate due to mutual interference, so it is recommended that users add LC filtering measures to the output of the DC/DC converter, as shown in Figure 43 below. The specific inductance capacity and capacitor capacity depend on the actual load of the user, please contact the manufacturer to negotiate;

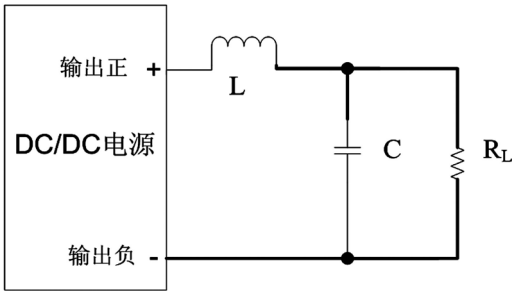


Figure 43 Schematic diagram of LC filtering

(16) When the DC/DC converter is used, it may be subject to external interference and oscillation, and the user should confirm the bus current waveform and the output voltage waveform of the DC/DC converter module to ensure that the circuit is in normal working condition.

(17) The DC/DC converter is hermetically sealed with high-purity nitrogen in a metal housing. When used in vacuum or low air pressure, it is normal for the upper cover to bulge slightly due to internal pressure. When the DC/DC converter is used, there should be at least 2 mm of space on the upper part to prevent the upper cover from being squeezed or short-circuited with other components when it is slightly bulging.