CDPM2758P

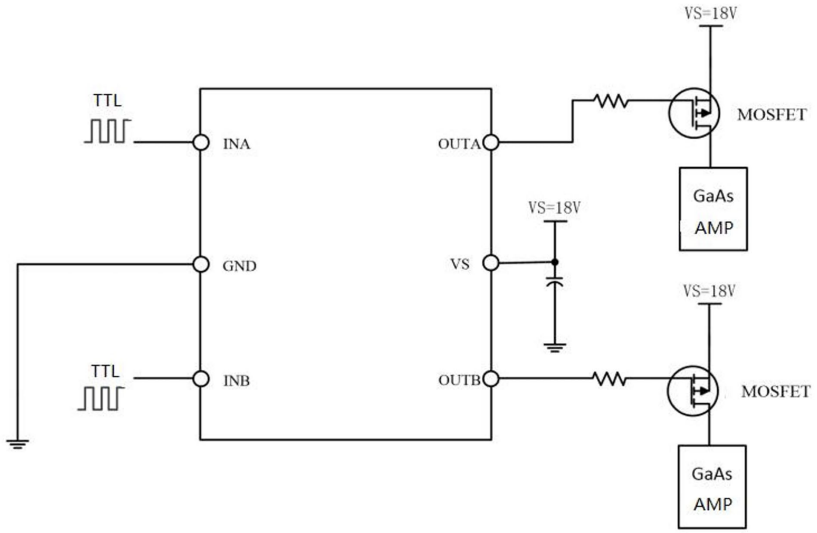
Drain Power Modulation

User guide

The traditional Circuit

Application:

- Power amplifier drain modulation
- TR component power modulation
- Phased array radar



Traditional solution:

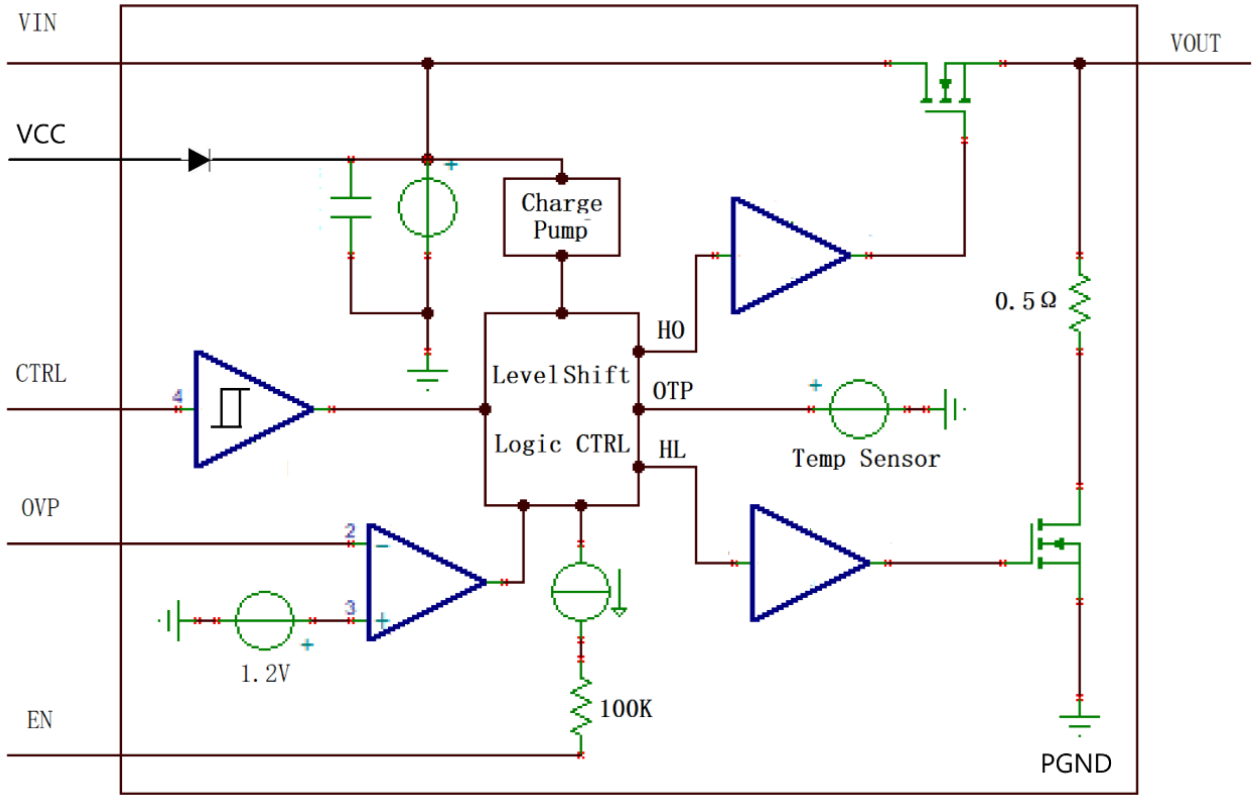
Driver + P&N-mosfet

MIC4426 driver

Disadvantage:

- PCB size unsuitable for TR
- Falling edge decided by load
- H-bridge： Continuous Mode Unsupported
- Enable logic need negative voltage detect
- Low frequency PWM because of Falling edge

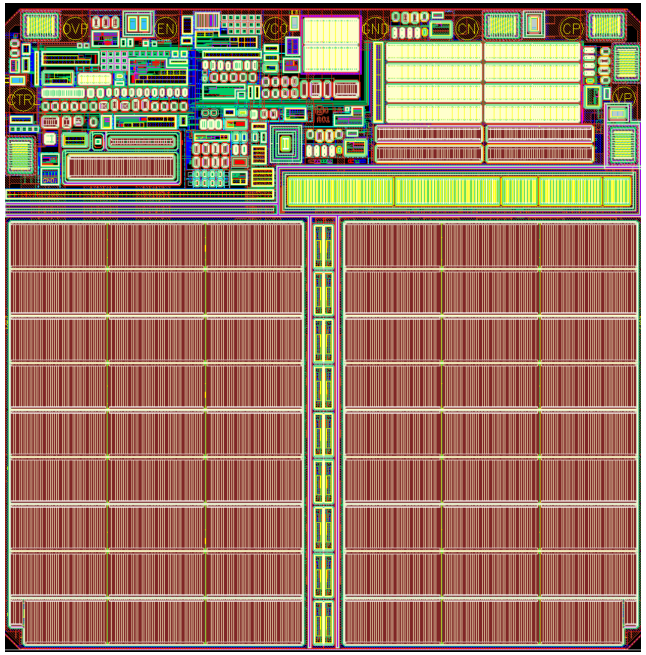
Our Solution

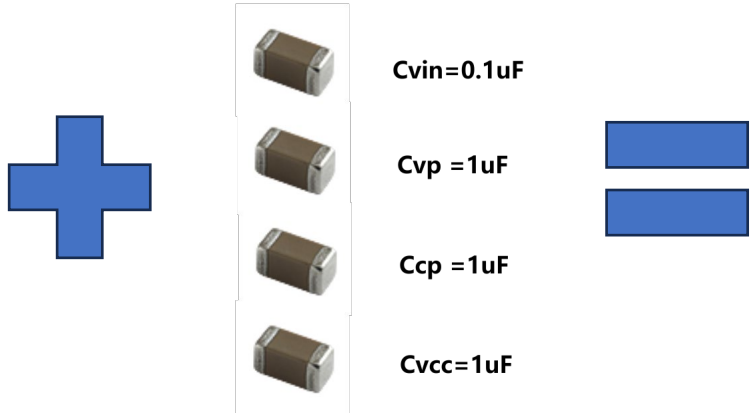


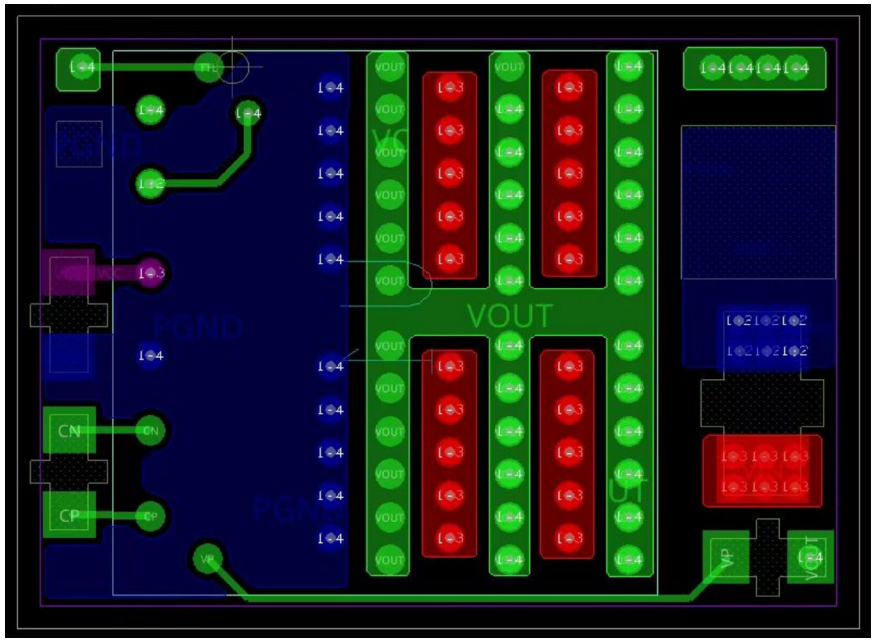
- Wide Input Voltage Range: 2.7V~58V
- Low Rdson : 18mΩ
- 7A DC, 8A Peak Output Current
- Pulse & Continuous Mode Supported
- Negitive Voltage Enable
- 5.5mm × 4.0mm × 0.9mm DFN20L Package

N-mosfet Integrated for High side and Low side
Charge Pump Inside supporte Continuous Mode

Substrate Flip chip Process





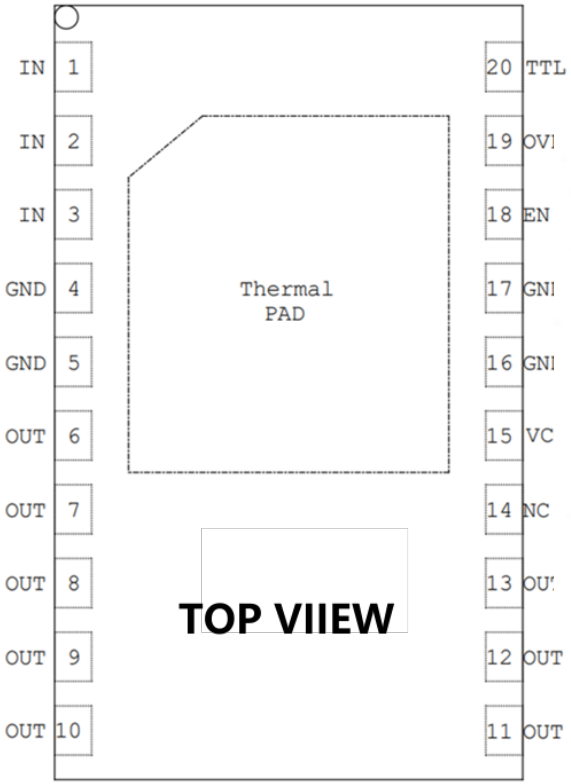


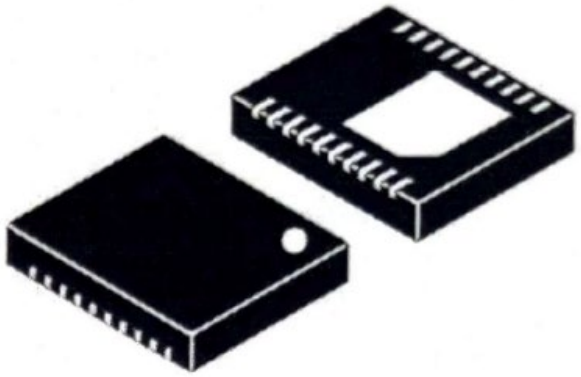
Load Switch Die

Charge Pump Cap

CDPM2758P

Functions

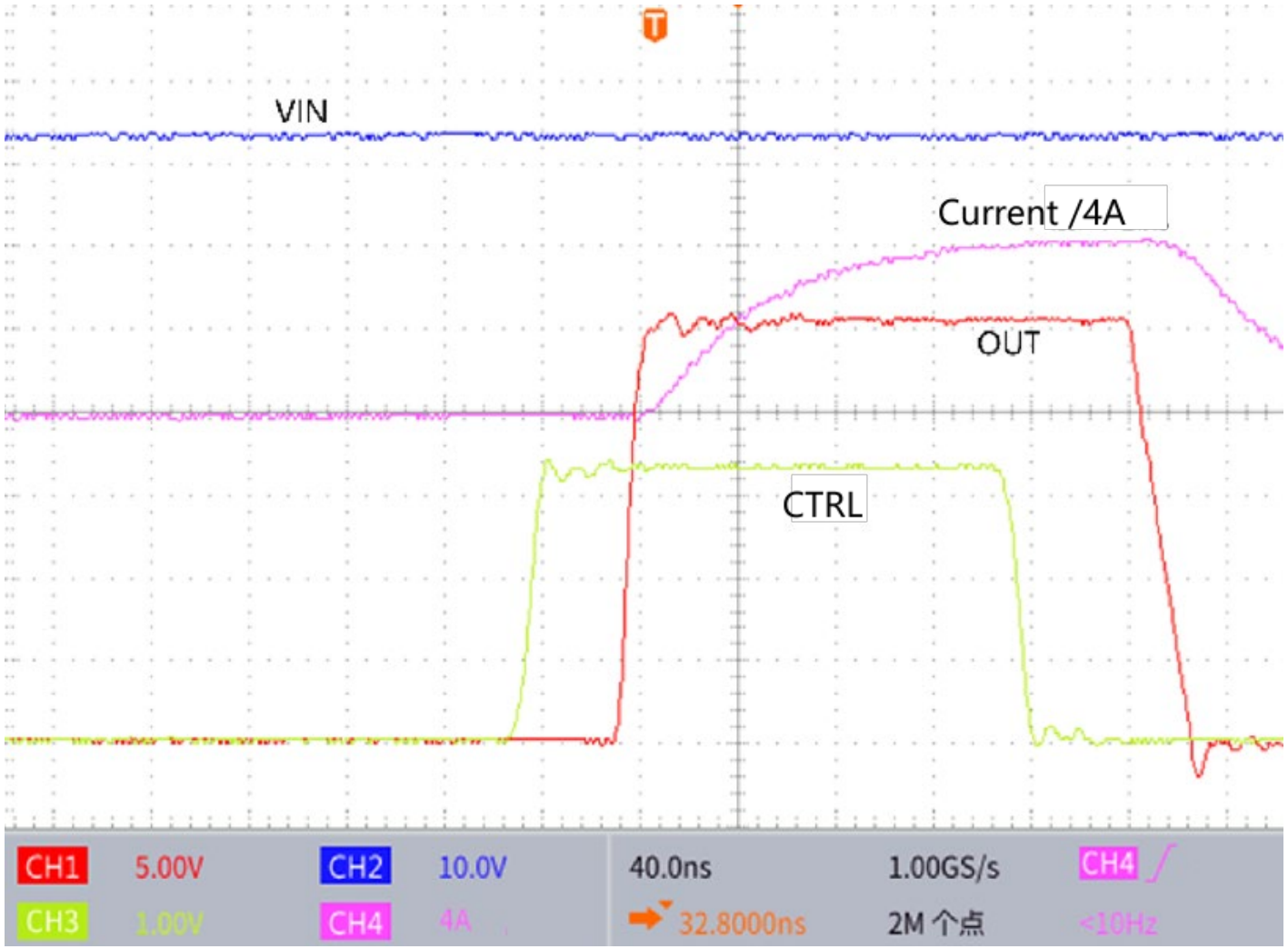




VIN	-	Power input
VOUT	-	Power output
GND	-	GND
NC	-	No connection
VCC	I	External VCC supply when VIN < 5V
EN	I	Negative Voltage enable
OVP	I	Over voltage protection,when ovp active, one-short protection : the device turn-off output until EN or VIN resuppled. Tied this pin to GND when no use. VOVP = 1.2*(RH+RL)/RL
CTRL	I	PWM signal input,when EN enable,output follows the pwm phase
EP	-	Thermal pad ,tied to GND and drill to GND plane by via to achive a better heat dissipation

Main Performance

Tr： 18ns Tf： 20ns, Tpg: 40ns Vin:2.7-58V Pulse： 8A, Continuous： 7A



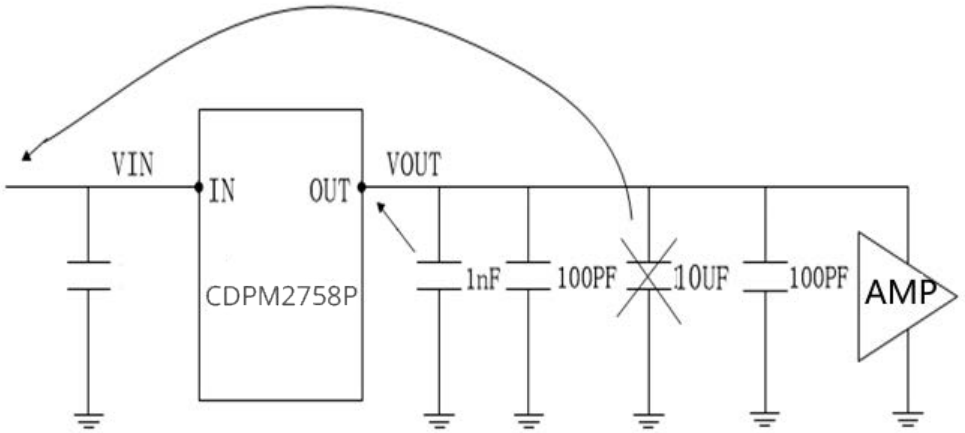
Application Note1

Cvin and Cout caps：

In order to meet the requirements of output top drop, in addition to the energy storage capacitor, there must be a ceramic capacitor Cvin near the input end, and Cvin must be 4000 times greater than the load capacitor. Additionally, there must be a 0.1uF decoupling capacitor near the VIN pin of CDPM2758P.

Due to the fact that the chip is designed for fast switching - charging and discharging external load capacitors, it is not recommended to exceed a maximum load capacitance of 10nF, which is also related to the switching frequency and input voltage. Detailed information on heat loss will be provided in subsequent chapters.

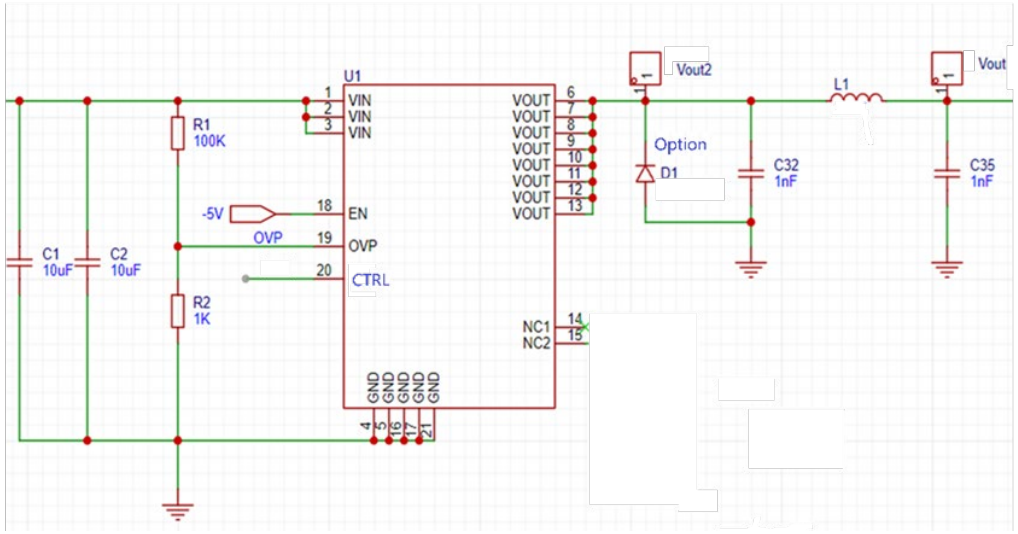
For power amplifiers with large matching capacitor requirements, it is recommended to place the large matching capacitor at the input end of the chip, leaving a 1-2nf level matching capacitor.Reduce the matchin inductance and the capacitance after matching inductance to avoid oscillation and self excitation.



Application Note2

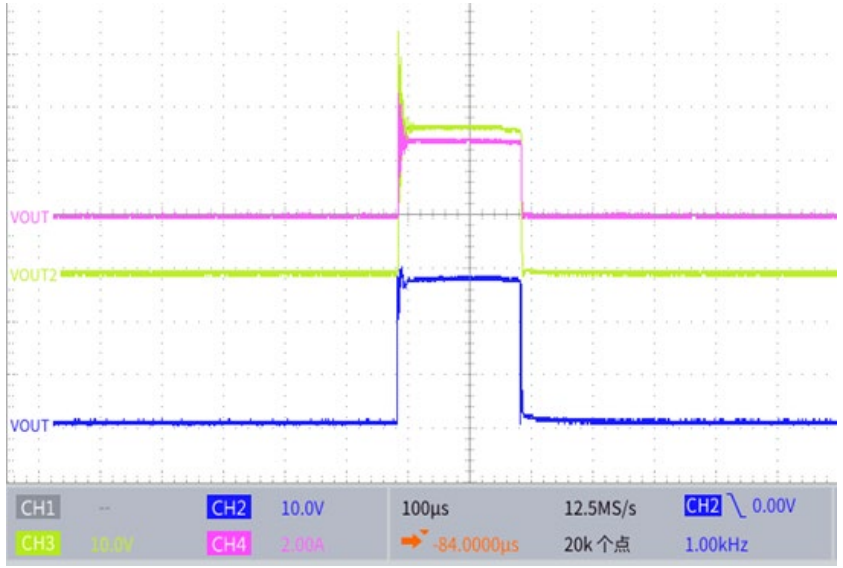
Cvin and Cout caps：

When the switching frequency is very low or in the case of continuous wave, the amplifier requires a large nearby capacitor, such as 1-10 uF level, which can be matched with inductance



You can choose a 10uH level inductor

to reduce output oscillation



L1= 10uH C35 = 1uF CH2

L1=0.68uH C35=1uF CH4

Application Note3

CTRL：

CTRL is the modulation control signal, and the chip has undergone 2ns level filtering processing internally. It is recommended that the system design handle this signal properly and follow the following rules:

Prohibit：

1）Do not use mechanical switches to control this pin, otherwise the output will oscillate with switch spikes, affecting the long-term reliability of the device.

2）Do not drive with negative output signal source, and do not drive CTRL signal voltage below -1.0V, as there is a risk of damaging the device.

Propose:

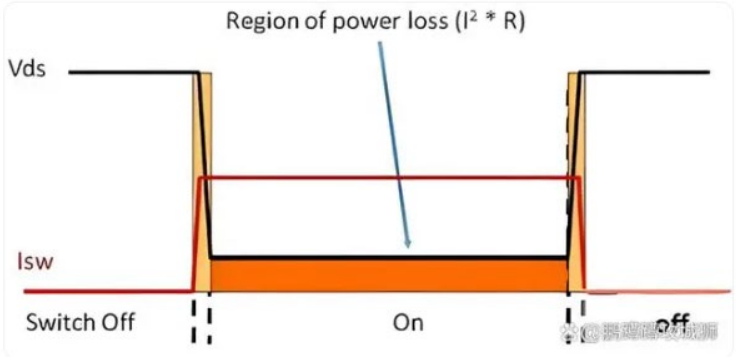
1) Use the shortest route and shield the wiring method to handle CTRL. Use GND holes to reflow near the CTRL wiring, as shown on the left in the figure below.
2) When VIN is greater than 36V, use a driver with driving capability to drive CTRL, such as 1G17 Schmitt driver gate circuit, and connect 5-22 Ω matching resistors in series to prevent reflection and avoid dv/dt interference with CTRL.

Application Note4

Power dissipation：

Power dissipation loss consists of three parts:1) GateDrive Loss PGC 2) Conduction Loss Pson 3) Switching Loss PSW PGC=n × VCC × Qg × fSW Because the driver is powered by an internal LDO, VCC=VIN, with built-in upper and lower tubes, n=2, Qg=2nc, and fSW is the CTRL frequency

The conduction loss Pson and switching loss PSW are shown in the figure on the right, where the switching time depends on the load capacitance Cout.Pson=I^2 * Rson * D, where Rson is the on resistance of CDPM2758P, approximately 12mΩ, and CDPM2758P, approximately 18mΩ,PSW = 1/2* fSW*Cout*VIN^2+ 1/2* fSW*Cout*VIN^2*E, Where E is the absorption coefficient E=RL/(RL+Roff) RL is the equivalent resistance of the load, and Roff is the internal resistance of the lower tube=50 ΩTherefore, the total chip loss Pd=PGC+Pson+PSW



Application Note5

Actual measurement of Power dissipation with no load：

Cout=1nF, D=50%	RL= 0			UNIT
fSW(KHz)	VIN=12V	VIN=28V	VIN=42	
10	6.8	7.8	8.6	
100	11.2	15.5	18.7	
200	16	23.9	29.8	
300	20.8	32.2	40.8	
400	25.6	40.6	51.5	
500	30.5	48.8	62.3	mA
600	35.1	57	73	
700	39.9	65		
800	44.5	73		
900	49.2	81.2		
1000	54	89.2		

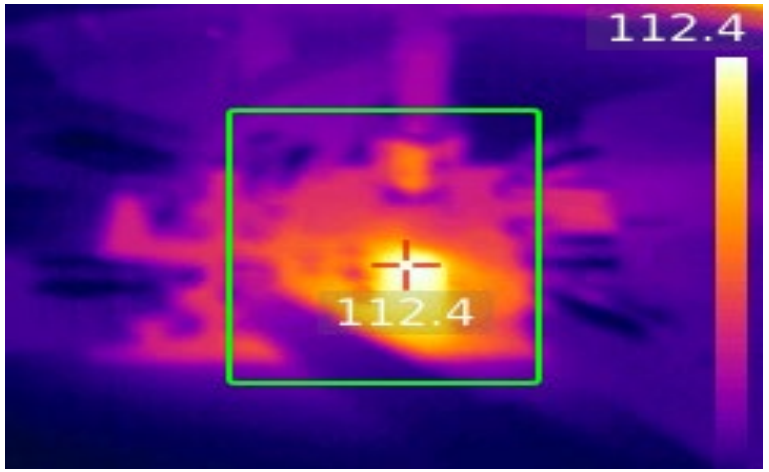
Cout=2nF, D=50%	RL= 0			UNIT
fSW(KHz)	VIN=12V	VIN=28V	VIN=42	
10	7	8.1	9.3	
100	12.6	18.6	23.5	
200	18.7	30.1	39.2	
300	24.9	41.7	54.6	
400	31	53.0	69.7	
500	37	64.2		mA
600	43.1	75.3		
700	49.1	86.4		
800	55.1	96.4		
900	61	107		
1000	67			

Power dissipation **is input voltage VIN × input current**

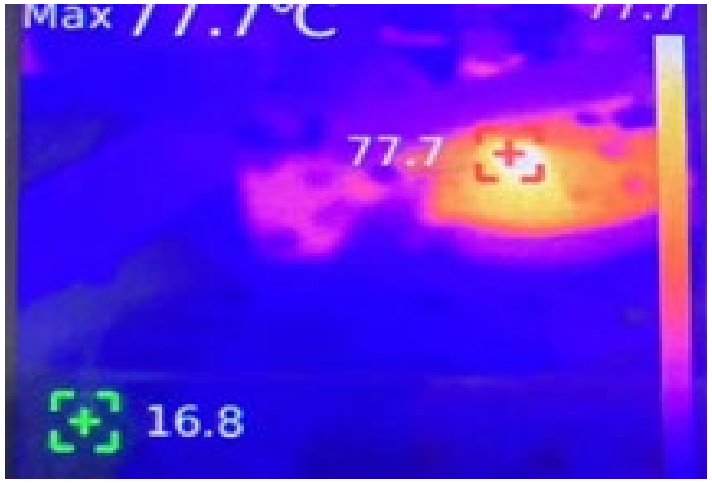
Application Note6

Thermal characteristic：

Vin=28V,Freq=1MHz,load=10R||3.3nF

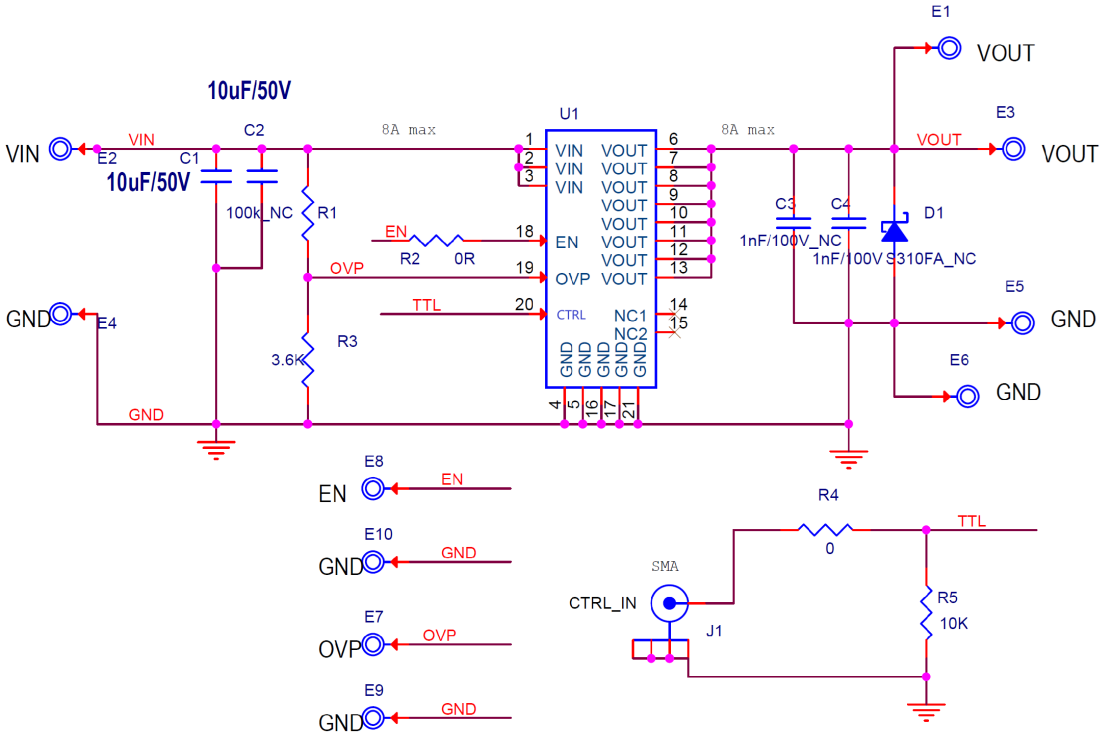


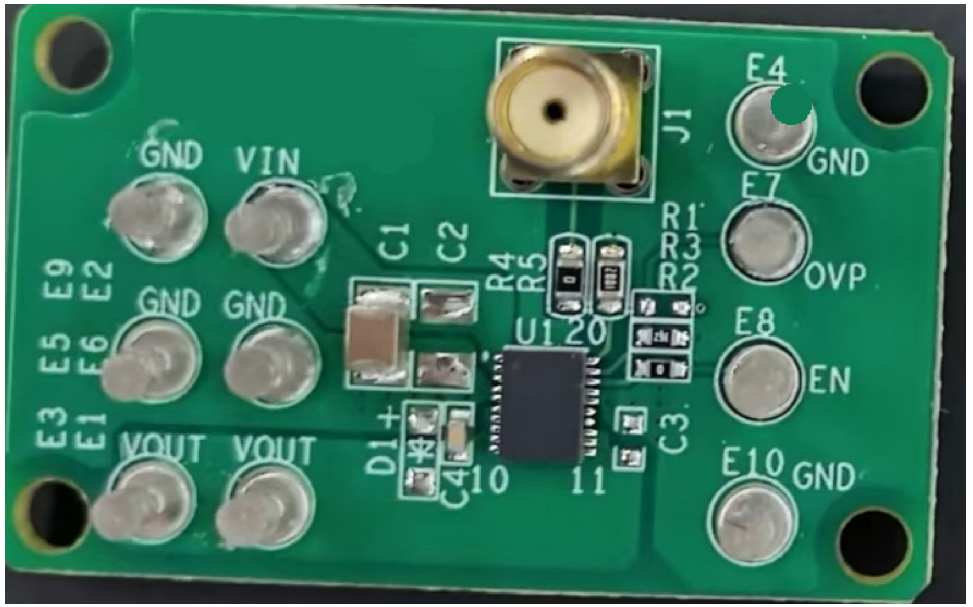
Vin=24V,freq=1MHz,duty=20%,iload=2A|| 2nF



Reduce output capacitance below 1nF level!
The circuit board has good heat dissipation!
Conditional top heat pad for heat dissipation!

DEMO KIT


10uF/50V
VIN
E2
C1
10uF/50V
C2
8A max
100k_NC
R1
EN
R2
0R
OVP
TTL
R3
3.6K
GND
E4
U1
VIN
VOUT
CTRL
NC1
NC2
GND
8A max
C3
C4
1nF/100V_NC
1nF/100V
D1
S310FA_NC
E1
VOUT
E3
VOUT
E5
GND
E6
GND
E8
EN
E10
GND
E7
OVP
E9
GND
R4
0
TTL
SMA
CTRL_IN
J1
R5
10K


GND
VIN
J1
E4
E7
GND
OVP
E8
EN
E10
GND
VOUT
VOUT
U1
20
11
C1
C2
C3
C4
R1
R2
R3
R4
R5
D1