User Instructions for BQ325RF256 device EVB

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Contents

1. Introduction

BQ325RF256 device EVB is a hardware platform designed for the use of BQ325RF256 RF integrated circuit, which can support the application and development of BQ325RF256 RF integrated circuit products. The EVB includes BQ325RF256 RF integrated circuit, supporting DDR3 high-speed storage applications, supporting PCIe2.0 interface, RS485 interface, 10/100/1000Mbps Ethernet interface and so on.

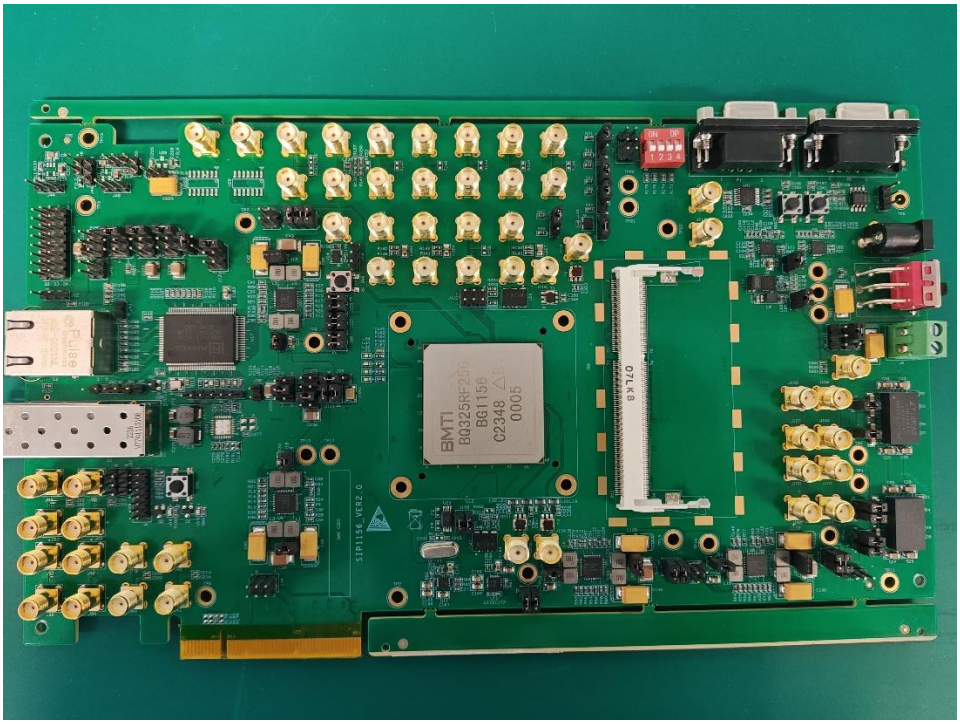


Figure 1 ： Top layer view of BQ325RF256 device EVB

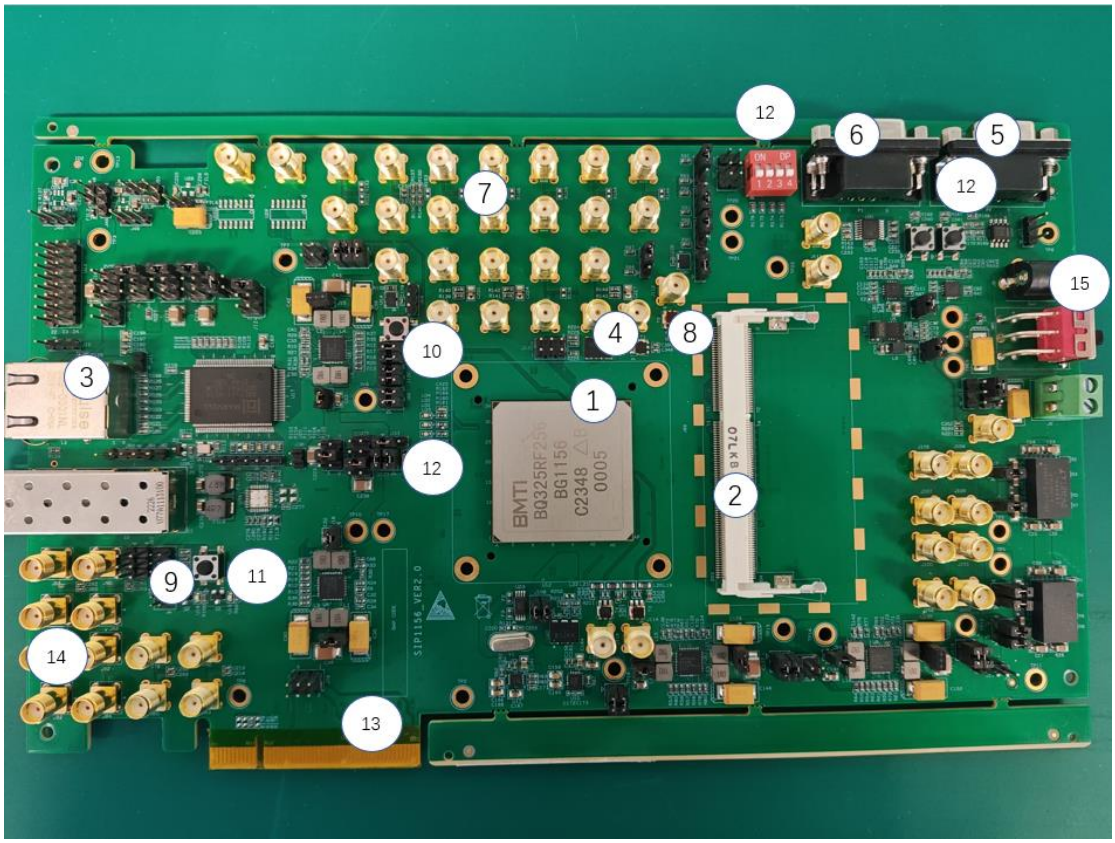
1.1Main features

- Memory: 1.5V DDR3 memory slot is configured on the FPGA end and supports MT8KTF51264HZ-1G9P1 memory with 4GB memory capacity.
- Clock and reset: Provides single-ended 80MHz, differential 200MHz clock input.
- Interface protocol: Support RS232/RS485 interface protocol.
- Configuration mode: Support JTAG online programming debugging, support the

built-in SPI Flash configuration.

- Dimensions: 266mm X 157mm
- Integrated RF transceiver function.

2. Detailed description of each part



1) BQ325RF256 RF integrated integrated circuit device

The device on the EVB is BQ325RF256 RF integrated integrated circuit.

The EVB supports JTAG configuration. Additionally, the FPGA can be configured using the built-in SPI flash.

2) 1.5V DDR3 memory slot

This EVB has a DDR3 memory slot connected to the FPGA end of the all-in-one circuit and can support MT8KTF51264HZ-1G9P1 memory with a 4GB memory capacity. The DDR3 pin definition mainly uses the BANK32, BANK33 and BANK34 corresponding to the FPGA.

Note: The constraints corresponding to FPGA XDC LOC are the XDC constraints during the creation of the project, not the real corresponding physical location of the chip. When using the board, you do not need to pay attention to the real physical location of the signal labeled on the schematic, but just follow the FPGA XDC LOC constraints to the corresponding pins.

For example: DDR3_A0 signal, the real physical location marked in the schematic is AP4, which corresponds to AB9 of the BQ7K325TFFG900 package, and the signal should be constrained to AB9 when establishing the constraints.

DDR3_SIGNAL	FPGA XDC LOC	FPGA BANK
DDR3_A0	AB9	BANK33
DDR3_A1	AB12	BANK33
DDR3_A2	AC10	BANK33
DDR3_A3	AC9	BANK33
DDR3_A4	Y10	BANK33
DDR3_A5	AA8	BANK33
DDR3_A6	AB10	BANK33
DDR3_A7	AA13	BANK33
DDR3_A8	AE9	BANK33
DDR3_A9	AA12	BANK33
DDR3_A10	AA11	BANK33
DDR3_A11	Y11	BANK33
DDR3_A12	AB8	BANK33
DDR3_A13	AA10	BANK33
DDR3_A14	AD8	BANK33
DDR3_A15	AE8	BANK33
DDR3_BA0	AC12	BANK33
DDR3_BA1	AC11	BANK33
DDR3_BA2	AD9	BANK33
DDR3_CAS_B	AG9	BANK33
DDR3_CKE0	AE10	BANK33
DDR3_CKE1	AF10	BANK33
DDR3_CLK0_N	AD11	BANK33
DDR3_CLK0_P	AD12	BANK33
DDR3_CLK1_N	AF11	BANK33

DDR3_CLK1_P	AE11	BANK33
DDR3_D0	AG19	BANK32
DDR3_D1	AH19	BANK32
DDR3_D2	AK19	BANK32
DDR3_D3	AJ19	BANK32
DDR3_D4	AD19	BANK32
DDR3_D5	AE19	BANK32
DDR3_D6	AF17	BANK32
DDR3_D7	AG18	BANK32
DDR3_D8	AA18	BANK32
DDR3_D9	AE18	BANK32
DDR3_D10	AB19	BANK32
DDR3_D11	AB18	BANK32
DDR3_D12	AD17	BANK32
DDR3_D13	AD18	BANK32
DDR3_D14	AC17	BANK32
DDR3_D15	AC19	BANK32
DDR3_D16	Y16	BANK32
DDR3_D17	AA17	BANK32
DDR3_D18	AD14	BANK32
DDR3_D19	AE15	BANK32
DDR3_D20	AA15	BANK32
DDR3_D21	AA16	BANK32
DDR3_D22	AB15	BANK32
DDR3_D23	AC14	BANK32
DDR3_D24	AJ17	BANK32
DDR3_D25	AK16	BANK32
DDR3_D26	AH15	BANK32

DDR3_D27	AK15	BANK32
DDR3_D28	AE16	BANK32
DDR3_D29	AH17	BANK32
DDR3_D30	AG15	BANK32
DDR3_D31	AG14	BANK32
DDR3_D32	AK8	BANK34
DDR3_D33	AJ8	BANK34
DDR3_D34	AK5	BANK34
DDR3_D35	AK4	BANK34
DDR3_D36	AF8	BANK34
DDR3_D37	AF7	BANK34
DDR3_D38	AG7	BANK34
DDR3_D39	AJ6	BANK34
DDR3_D40	AK3	BANK34
DDR3_D41	AJ3	BANK34
DDR3_D42	AJ1	BANK34
DDR3_D43	AK1	BANK34
DDR3_D44	AH6	BANK34
DDR3_D45	AH5	BANK34
DDR3_D46	AJ2	BANK34
DDR3_D47	AJ4	BANK34
DDR3_D48	AF2	BANK34
DDR3_D49	AF1	BANK34
DDR3_D50	AE1	BANK34
DDR3_D51	AF5	BANK34
DDR3_D52	AF6	BANK34
DDR3_D53	AG5	BANK34
DDR3_D54	AE5	BANK34

DDR3_D55	AE4	BANK34
DDR3_D56	AD3	BANK34
DDR3_D57	AC2	BANK34
DDR3_D58	AD4	BANK34
DDR3_D59	AC4	BANK34
DDR3_D60	AE6	BANK34
DDR3_D61	AD6	BANK34
DDR3_D62	AC5	BANK34
DDR3_D63	AC7	BANK34
DDR3_DM0	AF18	BANK32
DDR3_DM1	AB17	BANK32
DDR3_DM2	Y15	BANK32
DDR3_DM3	AF15	BANK32
DDR3_DM4	AK6	BANK34
DDR3_DM5	AH2	BANK34
DDR3_DM6	AE3	BANK34
DDR3_DM7	AC1	BANK34
DDR3_DQS0_N	AK18	BANK32
DDR3_DQS0_P	AJ18	BANK32
DDR3_DQS1_N	Y18	BANK32
DDR3_DQS1_P	Y19	BANK32
DDR3_DQS2_N	AC15	BANK32
DDR3_DQS2_P	AC16	BANK32
DDR3_DQS3_N	AJ16	BANK32
DDR3_DQS3_P	AH16	BANK32
DDR3_DQS4_N	AJ7	BANK34
DDR3_DQS4_P	AH7	BANK34
DDR3_DQS5_N	AH1	BANK34

DDR3_DQS5_P	AG2	BANK34
DDR3_DQS6_N	AG3	BANK34
DDR3_DQS6_P	AG4	BANK34
DDR3_DQS7_N	AD1	BANK34
DDR3_DQS7_P	AD2	BANK34
DDR3_ODT0	AK10	BANK33
DDR3_ODT1	AH11	BANK33
DDR3_RAS_B	AK9	BANK33
DDR3_RESET_B	AE13	BANK33
DDR3_S0_B	AH9	BANK33
DDR3_S1_B	AK11	BANK33
DDR3_TEMP_EVENT_B	AJ11	BANK33
DDR3_WE_B	AJ9	BANK33
SYSCLK_N	AH10	BANK33
SYSCLK_P	AG10	BANK33

3) Ethernet interface

This EVB has a 10/100/1000Mbps Ethernet port connected to the FPGA end of the all-in-one circuit.

4) Clock resources

This development board has a differential 200MHz active crystal input, and a single-ended 80MHz active crystal.

CLOCK NAME	SIGNAL	FPGA XDC LOC	DESCRIPTION
SYSCLK_200	SYSCLK_200_N	AC27 （bank13）	200MHz differential pair
	SYSCLK_200_P	AB27 （bank13）	
FPGA_CLK80	FPGA_CLK80	AE28 （bank13）	80MHz single-ended

Also, 1 pair of differential clock SMA inputs is supported.

CLOCK NAME	SIGNAL	FPGA XDC LOC	DESIGNATOR
SYSCLK_SMA	SYSCLK_SMA_N	AH29 （bank13）	J60

	SYSCLK_SMA_P	AG29 （bank13）	J62

5) **RS485**

This board contains a female DB9 RS485 serial port that allows the FPGA to transfer data with other devices. When in use, just connect an external serial cable.

SIGNAL NET	DIRECTION	FPGA XDC LOC
RS485_R	R	G19
RS485_RE	ENABLE of R	C20
RS485_D	T	E18
RS485_DE	ENABLE of T	A22

6) **RS232**

This board contains a female DB9 RS232 serial port that allows the FPGA to transfer data with other devices. When in use, just connect an external serial cable.

SIGNAL NET	DIRECTION	FPGA XDC LOC
FPGA_RS232_TX	T	A16
FPGA_RS232_RX	R	A17

7) **User-available extended IO**

This EVB supports differential IO for different voltage standards.

NET	DESIGNATOR	BANK	VOLTAGE	FPGA XDC LOC
BANK17_1_P	J63	17	1.8V/2.5V/3.3V	K18
BANK17_1_N	J65	17	1.8V/2.5V/3.3V	J18
BANK17_11_P_SRCC	J69	17	1.8V/2.5V/3.3V	F21
BANK17_11_N_SRCC	J73	17	1.8V/2.5V/3.3V	E21
BANK17_12_P_MRCC	J70	17	1.8V/2.5V/3.3V	F20
BANK17_12_N_MRCC	J74	17	1.8V/2.5V/3.3V	E20
BANK17_7_P	J64	17	1.8V/2.5V/3.3V	H21
BANK17_7_N	J66	17	1.8V/2.5V/3.3V	G13
BANK17_15_P	J75	17	1.8V/2.5V/3.3V	D16
BANK17_15_N	J76	17	1.8V/2.5V/3.3V	C16
BANK17_17_P	J67	17	1.8V/2.5V/3.3V	C17
BANK17_17_N	J71	17	1.8V/2.5V/3.3V	B17
BANK17_21_P	J68	17	1.8V/2.5V/3.3V	A20
BANK17_21_N	J72	17	1.8V/2.5V/3.3V	A21
BANK33_20_P	J100	33	1.5V	AK14
BANK33_20_N	J102	33	1.5V	AK13
BANK33_21_P	J101	33	1.5V	AH14
BANK33_21_N	J103	33	1.5V	AJ14
BANK33_22_P	J104	33	1.5V	AJ13
BANK33_22_N	J106	33	1.5V	AJ12
BANK33_23_P	J105	33	1.5V	AF12
BANK33_23_N	J107	33	1.5V	AG12

8) Rf transceiver interface

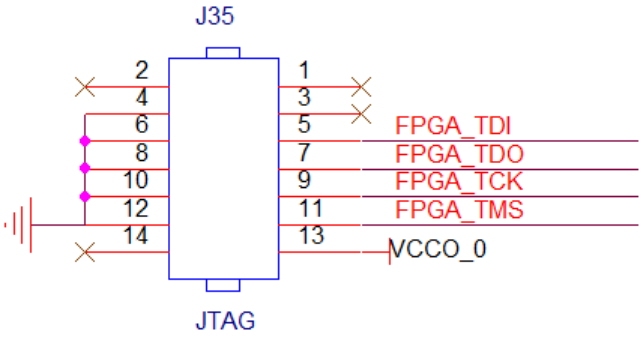
This development board integrates the RF module B9361, which can realize the RF transceiver function after configuring the 9361 through FPGA. The interconnection relationship between RF module and FPGA module and the XDC constraint position of FPGA are shown in the following table. When porting the routines, it is necessary to pay attention to change the XDC constraint position. The level standard of the interconnection signal between the RF module and the FPGA is 2.5V by default.

FPGA_SIGNAL_NET	RF_SIGNAL_NET	FPGA XDC LOC
I/O_L24P_T3_12	P1_D7/RX_D3_P	AK20
I/O_L22P_T3_12	P1_D5/RX_D2_P	AG20
I/O_L24N_T3_12	P1_D6/RX_D3_N	AK21
I/O_L22N_T3_12	P1_D4/RX_D2_N	AH20
I/O_L20P_T3_12	P1_D3/RX_D1_P	AG22
I/O_L20N_T3_12	P1_D2/RX_D1_N	AH22
I/O_L18P_T2_12	P1_D1/RX_D0_P	AG25
I/O_L18N_T2_12	P1_D0/RX_D0_N	AH25
I/O_L16P_T2_12	P0_D11/TX_D5_P	AE25
I/O_L16N_T2_12	P0_D10/TX_D5_N	AF25
I/O_L14P_T2_SRCC_12	P0_D9/TX_D4_P	AG24
I/O_L14N_T2_SRCC_12	P0_D8/TX_D4_N	AH24
I/O_L23P_T3_12	P0_D7/TX_D3_P	AH21
I/O_L23N_T3_12	P0_D6/TX_D3_N	AJ21
I/O_L21P_T3_DQS_12	P0_D5/TX_D2_P	AJ22
I/O_L21N_T3_DQS_12	P0_D4/TX_D2_N	AJ23
I/O_L19P_T3_12	P0_D3/TX_D1_P	AF20
I/O_L19N_T3_VREF_12	P0_D2/TX_D1_N	AF21
I/O_L17P_T2_12	P0_D1/TX_D0_P	AK23
I/O_L17N_T2_12	P0_D0/TX_D0_N	AK24
I/O_L12N_T1_MRCC_12	FB_CLK_N	AE24
I/O_L12P_T1_MRCC_12	FB_CLK_P	AD23
I/O_L11N_T1_SRCC_12	DATA_CLK_N	AF23
I/O_L11P_T1_SRCC_12	DATA_CLK_P	AE23
I/O_L9N_T1_DQS_12	TX_FRAME_N	AD24
I/O_L9P_T1_DQS_12	TX_FRAME_P	AC24
I/O_L7N_T1_12	RX_FRAME_N	AC25
I/O_L7P_T1_12	RX_FRAME_P	AB24
I/O_L5N_T0_12	SYNC_IN	AC21
I/O_L3N_T0_DQS_12	TXNRX	AB23
I/O_L1N_T0_12	EN_AGC	Y24
I/O_L10N_T1_12	ENABLE	AE21
I/O_L8N_T1_12	CTRL_OUT7	AD22
I/O_L6N_T0_VREF_12	CTRL_OUT5	AB20
I/O_L4N_T0_12	CTRL_OUT6	AA23

I/O_L2N_T0_12	CTRL_OUT4	AA21
I/O_0_12	CTRL_OUT2	Y20
I/O_L5P_T0_12	CTRL_OUT3	AC20
I/O_L3P_T0_DQS_12	CTRL_OUT0	AB22
I/O_L1P_T0_12	CTRL_OUT1	Y23
I/O_L4P_T0_12	CTRL_IN2	AA22
I/O_L2P_T0_12	CTRL_IN3	Y21
I/O_L10P_T1_12	CTRL_IN1	AD21
I/O_L8P_T1_12	CTRL_IN0	AC22
I/O_L24P_T3_13	SPI_CLK	AJ26
I/O_L22P_T3_13	SPI_DI	AH26
I/O_L20P_T3_13	SPI_DO	AJ27
I/O_L18P_T2_13	SPI_ENB	AG30
I/O_L15P_T2_DQS_12	P1_D11/RX_D5_P	AJ24
I/O_L6P_T0_12	CLK_OUT	AA20
I/O_L15N_T2_DQS_12	P1_D10/RX_D5_N	AK25
I/O_L13P_T2_MRCC_12	P1_D9/RX_D4_P	AF22
I/O_L13N_T2_MRCC_12	P1_D8/RX_D4_N	AG23
I/O_25_12	RESETB	AE20

9) JTAG

This EVB can be configured with the FPGA end through the JTAG configuration interface.



10)SPI Flash

The all-in-one circuit has a built-in 256Mbit SPI FLASH and supports X1/X2/X4 modes. To use it in VIVADO, select MX25L25645G-SPI-X1_X2_X4, and also configure the configuration pins [M2:M0] to [001].

11)DONE and INIT LEDs

U16 INIT lights when the FPGA is powered up and initialized successfully. U15 DONE lights when the FPGA is successfully configured.

12)GPIO

This development board provides four user-available LEDs connected to the FPGA general-purpose IOs.

LED NET	DESIGNATOR	FPGA XDC LOC
GPIO_LED_0	U32	G22（bank17）

GPIO_LED_1	U33	F22（bank17）
GPIO_LED_2	U34	D22（bank17）
GPIO_LED_3	U35	C22（bank17）

This development board has two user-available keys connected to the FPGA general-purpose IOs, which are high by default and low when pressed, with the following location constraints:

DESIGNATOR	NET	FPGA XDC LOC
SW3	GPIO_SW_0	L18（bank17）
SW4	GPIO_SW_1	K19（bank17）

This development board has 4 dip switches connected to the FPGA general purpose IOs. The default is low, and the toggle code to the ON position is high.

DIP_SW NET	DESIGNATOR	FPGA XDC LOC
GPIO_DIP_SW0	SW5	D17（bank17）
GPIO_DIP_SW1		D18（bank17）
GPIO_DIP_SW2		E19（bank17）
GPIO_DIP_SW3		D19（bank17）

13)PCIe

This development board has a PCIe slot that connects to the FPGA side of the integrated circuit and supports PCIe 2.0x8 rates. GTX BANK 115 and 116 are used.

14)GTX IO

This development board provides 2 pairs of GTX receive differential pair SMAs, 2 pairs of GTX transmit differential pair SMAs, and 1 pair of GTX clock resource SMAs. these 5 pairs of signals occupy BANK118.

	SIGNAL NET	DESIGNATOR	Location	FPGA XDC LOC
SMA0_TX	MGTXTXP0_118	J82	GTXE2_CHANNEL _X0Y12	D2
	MGTXTXN0_118	J84		D1
SMA1_TX	MGTXTXP1_118	J87	GTXE2_CHANNEL _X0Y13	C4
	MGTXTXN1_118	J89		C3
SMA0_RX	MGTXRXP0_118	J83	GTXE2_CHANNEL _X0Y12	E4
	MGTXRXN0_118	J85		E3
SMA1_RX	MGTXRXP1_118	J88	GTXE2_CHANNEL _X0Y13	D6
	MGTXRXN1_118	J90		D5
MGTREFCLK	MGTREFCLK0P_118	J79	GTXE2_COMMON _X0Y3	C8
	MGTREFCLK0N_118	J80		C7

15)Power Supply

J9 can choose to be powered by a power adapter or otherwise external power supply. The power adapter can be DC12V (compatible with DC5V).

NET NAME	VOLTAGE	JUMPER
VCC_5V_1	5V	J1 J3
VCC_5V_2	5V	J2 J4
VCC_2V5	2.5V	J6 J7
VCC_INT_1V0	1.0V	J15 J16

VCC_BRAM_1V0	1.0V	J22
VCC_IO_1V8	1.8V	J17
VCC_IO	2V	J18
VCC_3V3	3.3V	J24
VCC_MGTAVCC_1V0	1.0V	J21
VCC_MGTAVTT_1V2	1.2V	J23
VCC_0V75	0.75V	
VCC_1V3	1.3V	

Selection of each voltage supplied to the chip side is shown in the table below.

VCC_INT	1.0V	J118
VCC_BRAM	1.0V	J119
VCC_AUX	1.8V	J120
VCC_AUX_IO_G0	1.8V	J121
VCC0_0	1.8V/2.5V/3.3V	J27
VCCO_12	1.8V/2.5V	J123
VCCO_13	1.8V/2.5V/3.3V	J61
VCCO_14	1.8V/2.5V/3.3V	J26
VCC0_15	1.8V/2.5V/3.3V	J28
VCCO_16	2.5V/3.3V	2V5RO3V1
VCCO_17	1.8V/2V/2.5V/3.3V	J77
VCCO_18	1.8V/2.5V/3.3V	J124
VCCO_32/33/34	1.5V	J108
VCC_3V3_9364	3.3V	J19
VCC_2V5_9364	2.5V	J20
VCC_SPI	3.3V	J109

3. Apply precautions

1. External power input can use 12V or 5V power supply.
2. FPGA side through the general-purpose IO and 9361 configuration signals in the RF integrated circuit internal interconnection, you can configure the 9361 through the FPGA and realize the RF transceiver functions.
3. integrated circuit built-in SPI Flash, burn in the vivado select "MX25L25645G-SPI-X1_X2_X4".
4. It is recommended to use an external clock source for the reference clock of the RF module. The silkscreen on the board is J115.

4.Help and support

Each part of the EVB has been simply tested before leaving the factory. If you have any

questions during use, you can contact us.
contact details:
contact address: No. 2, Siyingmen North Road, Donggaodi, Fengtai District, Beijing
Postal code: 100076
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