

РАБОТА С ОТЛАДОЧНОЙ ПЛАТОЙ ZF-706

на основе ПЛИС Fudan

FMQL45T900

A decorative graphic consisting of several parallel white lines of varying thicknesses, slanted diagonally from the bottom-left towards the top-right, set against a blue gradient background.

СОСТАВ ОТЛАДОЧНОЙ ПЛАТЫ ZF-706

- ▶ Fudan FMQL45T900 (4xCortex-A7, 256Кб L2, 256Кб SRAM, 218k LUTs, 437k FFs, 19,2 Мбит BRAM, 900 МАСС18x25, 2 ADC)
- ▶ Конфигурационное ПЗУ QSPI 256 Мбит
- ▶ Генераторы 50 МГц(PS), 33 МГц(PL)
- ▶ 1 Гбайт DDR3-1066 PS, 2 Гбайт DDR3-1066 PL
- ▶ 1Gb Ethernet (PHY LAN88E1116 RGMII)
- ▶ HDMI-выход (1080p @ 60 Гц)
- ▶ USB-UART PS(CP2102), USB-UART EMIO (CP2102), USB2.0(USB3320C)
- ▶ Интерфейс SD-card
- ▶ Интерфейс PCIe x8
- ▶ Встроенный программатор USB-JTAG (совместим с Digilent)

ВНЕШНИЙ ВИД ОТЛАДОЧНОЙ ПЛАТЫ ZF-706

JTAG PS

User I/O

SD-card

USB

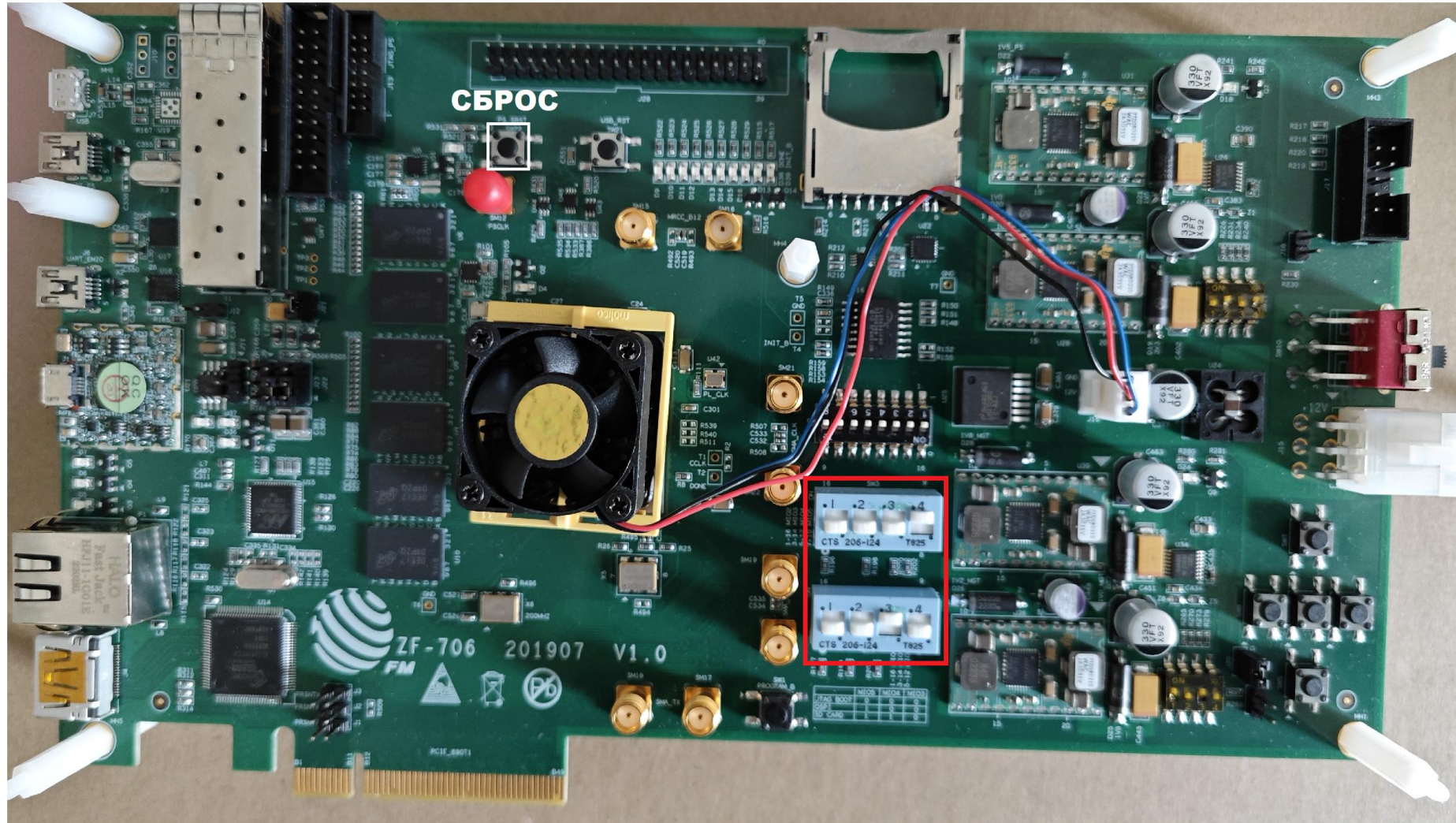
UART PS

UART EMIO

JTAG PL

Ethernet

HDMI



Вкл. питания

разъем БП
12 В (5 А)

ОСОБЕННОСТИ ПЛИС FMQL45T900

- ▶ Необходимость учитывать перенос некоторых сигналов на другие выходы и межсоединения относительно аналога Xilinx (SD_CDn, SRAM_BLS_B, CPU_IRQ)
- ▶ Отсутствие арбитража и управления потоком (handshake/flow control) DMA-транзакций между PS и PL
- ▶ Необходимость учитывать отличия в DDR-контроллере (контакты VRN/VRP)
- ▶ 4 ядра ARM Cortex-A7 вместо 2-х Cortex-A9
- ▶ Кэш L2 объемом 256 Кбайт вместо 512 Кбайт
- ▶ Работа с СнК в САПР Procise 2023.1 и IAR Embedded Workbench for ARM 8.11.2
- ▶ Работа с ПЛИС в САПР Procise 2023.1 или Vivado 2018.3
- ▶ Необходимость учитывать особенности ПЛИС при работе в Vivado 2018.3

ОСОБЕННОСТИ РАБОТЫ С ОТЛАДОЧНОЙ ПЛАТОЙ

- ▶ Работа в Vivado 2018.3 с ПЛИС осуществляется через Digilent-совместимый программатор распаянный на плате (JTAG PL)
- ▶ Работа с СнК и ПЛИС в ProCise 2023.1 и IAR 8.2.11 осуществляется через программатор J-link V9 (Jlink firmware ver. 9.70; Jlink driver ver. 6.50a)
- ▶ При отладке проекта в IAR необходимо переводить СнК в режим загрузки через JTAG, иначе СнК будет загружаться с SD/QSPI, что приведет к конфликту при отладке
- ▶ В начале работы необходимо проверить и правильно выставить перемычки (джамперы) и микропереключатели согласно описанию на отладочную плату

PROGRAMMABLE CIRCUIT AND SYSTEM COMPILER (PROCISE 2023.1)

The screenshot displays the PROCISE 2023.1 software interface. The main window shows a Verilog HDL code editor with the following code:

```
1 `timescale 1ns / 1ps
2
3 module led_procise (
4     input sys_clk,
5     output reg [7:0] led
6 );
7 reg[31:0] timer_cnt;
8 reg[7:0] led_cnt;
9
10 always@(posedge sys_clk)
11 begin
12     if(timer_cnt >= 32'd24_999_999)
13     begin
14         led_cnt <= led_cnt + 8'd1;
15         timer_cnt <= 32'd0;
16     end
17     else
18     begin
19         led <= led_cnt;
20         timer_cnt <= timer_cnt + 32'd1;
21     end
22 end
23 endmodule
24
```

The left sidebar shows the project hierarchy and the Run FPGA flow process. The bottom panel shows the TCL Console with the following output:

```
-- Analyzing Verilog file F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/sources/led_procise.v (VERI-1704)
read_phy_design F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/rundir/.9ae7ce383269ad0c458c98fda6b5f19.phy
Read FDC F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/rundir/led_procise_placed.fdc
load_design elapsed_time 0.68 seconds, cpu_time 0.78 seconds
load_design used memory 5MB, procise used peak memory 962MB, current used memory 855MB

DiffDupPass : total create 0 insts for model 'layout'
HfsPass : total split 0 nets for model 'layout'
DiffDupPass : total create 0 insts for model 'layout'
Phase 1.1.6 Build Placer Netlist Model
Phase 1.1.6 Build Placer Netlist Model | Time: 1.71387e+009s
init IO Planning data succeed.
```

The status bar at the bottom indicates "Console" with "No error" and "No warning" messages.

PROCISE 2023.1 - F:/WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/led_procise.fpe - [Project Tabs]

Project Source Tools ESOE Window Help

Start

Hierarchy

- Sources
 - led_procise (led_procise.v)
- Constraints
 - constrs_1
 - led_procise.ucf (Active) (led_proc
- Simulation

Run FPGA flow

Current stage: Post-Sitgen

Processes

- Project Summaries
- IP
 - IP Catalog
- Block Design
 - Create Block Design
 - Open Block Design
- Design Utilities
 - View Command Line Log
 - Elaborate
 - Synthesize
 - View Post-Synthesize Timing Summary
 - Generate Post-Synthesize Simulation File
 - Implement Design
 - Place
 - View Post-Place Timing Summary
 - Route
 - View Post-Route Timing Summary
 - Generate Bitstream
 - Configure Device
 - Create FROM File
 - Program Device
 - ChipXplorer Analyzer

F:/WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/constraints/constrs_1/led_procise.ucf

```
1 NET "led[0]" IOSTANDARD = LVCMOS33;
2 NET "led[1]" IOSTANDARD = LVCMOS33;
3 NET "led[2]" IOSTANDARD = LVCMOS33;
4 NET "led[3]" IOSTANDARD = LVCMOS33;
5 NET "led[4]" IOSTANDARD = LVCMOS33;
6 NET "led[5]" IOSTANDARD = LVCMOS33;
7 NET "led[6]" IOSTANDARD = LVCMOS33;
8 NET "led[7]" IOSTANDARD = LVCMOS33;
9 NET "led[0]" LOC = AJ25;
10 NET "led[1]" LOC = AK22;
11 NET "led[2]" LOC = AJ21;
12 NET "led[3]" LOC = AJ23;
13 NET "led[4]" LOC = AH23;
14 NET "led[5]" LOC = AD24;
15 NET "led[6]" LOC = AG22;
16 NET "led[7]" LOC = AF23;
17
18 NET "sys_clk" LOC = AE22;
19 NET "sys_clk" IOSTANDARD = LVCMOS33;
20 TIMESPEC TS_SYS_CLK = PERIOD "sys_clk" 50 MHz HIGH 50 %;
21
```

Project Summaries x led_procise.ucf x

TCL Console

```
Build time : 2024/04/23 18:21:10
Start time : 2024-04-23 18:19:39
>>set_device fmq145t900
set_device elapsed_time 8.66 seconds, cpu_time 9.00 seconds
set_device used memory 892MB, procise used peak memory 967MB, current used memory 697MB

>>load_design -stage_post_map -no_hier
-- Analyzing Verilog file 'F:/WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/sources/led_procise.v' (VERI-1482)
read_phy_design F:/WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/rundir/.9ae7ce383269ad0c458c98fcdab5f19.phy
Read FDC F:/WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/rundir/led_procise_placed.fdc
load_design elapsed_time 0.66 seconds, cpu_time 0.77 seconds
load_design used memory 10MB, procise used peak memory 967MB, current used memory 727MB

Command>
```

Project Design Files

Console No error No warning

ЗАГРУЗКА ПРОГРАММЫ В ПЛИС ЧЕРЕЗ JTAG

The screenshot displays the Xilinx Vivado IDE interface. The 'Tools' menu is open, with 'I/O Planning' selected. The main editor shows the Verilog code for the 'led_procise' module. The TCL Console at the bottom shows the output of the 'read_phy_design' command, indicating that the design has been read successfully and IO planning data has been initialized.

```
golden_demo/ch2_ledp/led_procise/sources/led_procise.v
le 1ns / 1ps

led_procise(
    sys_clk,
    at_reg [7:0] led

    timer_cnt;
    led_cnt;

posedge sys_clk)

timer_cnt >= 32'd24_999_999)
led_cnt <= led_cnt + 8'd1;
timer_cnt <= 32'd0;

led <= led_cnt;
timer_cnt <= timer_cnt + 32'd1;
end
endmodule
endmodule
endmodule
endmodule
```

```
TCL Console
-- Analyzing verilog file F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/sources/led_procise.v (1621-1704)
read_phy_design F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/rundir/.9ae7ce383269ad0c458c98f0da6b5f19.phy
Read FDC F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/rundir/led_procise_placed.fdc
load_design elapsed_time 0.68 seconds, cpu_time 0.78 seconds
load_design used memory 5MB, procise used peak memory 962MB, current used memory 855MB

DiffDupPass : total create 0 insts for model 'layout'
HfsPass : total split 0 nets for model 'layout'
DiffDupPass : total create 0 insts for model 'layout'
Phase 1.1.6 Build Placer Netlist Model
Phase 1.1.6 Build Placer Netlist Model | Time: 1.71387e+009s
init IO Planning data succeed.

Command>
```


ЗАГРУЗКА ПРОГРАММЫ В ПЛИС ЧЕРЕЗ JTAG

The screenshot displays the PROCISE - Program software interface. The main window is titled "Chain configuration of your board" and shows a diagram of the JTAG chain with two FMSH (FPGA Master Slave) components: "ps_dap bypass" and "fmq45 bypass". The TDI and TDO lines are connected to these components. Below the diagram, the TAP_num and IR Length values are listed:

TAP_num	1	0
IR Length	4bit	6bit

The console window at the bottom shows the following output:

```
>>init_chain -cable_type jlink
hw_server: Jlink firmware version: 9.70
hw_server: Jlink driver version: 6.50a
hw_server: Select Device Successfully
hw_server: Set Jlink speed to 6000khz failed
hw_server: Current Jlink speed is 65534khz
hw_server: Jlink speed is already 6000khz
hw_server: JTAG tap: Procise found HwServer chain_info: 0x03731093 (mfg:0x049(FMSH), part:0x3731(jfm7z045), ver:0x0)
hw_server: read rsvd_req_7
hw_server: read rsvd value 0x00000000 !

hw_server: JTAG tap: Procise found HwServer chain_info: 0x4ba00477 (mfg:0x23b(ARM), part:0xba00(arm_dap), ver:0x4)
-----
device_id: 00000011011100110001000010011011
manufacturer: FMSH
part_name: fmq45
part_id: 0
ir_length: 6
version: 0
step_id: 0
-----
device_id: 0100101110100000000010001110111
manufacturer: FMSH
part_name: ps_dap
part_id: 1
ir_length: 4
version: 0
step_id: 0
hw_server: SVF instructions execute success
init_chain elapsed_time 2.77 seconds, cpu_time 0.17 seconds
init_chain used memory 1MB, procise used peak memory 962MB, current used memory 875MB
```

Identify Succeeded

PROCISE - Program

File View Window Psoc Tools Help

Main

- Connect to board
- Create PROM File

Cables

Cable	Status
SEGGER...	Connected

Chain configuration of your board

Program

- Access eFUSE Registers
- Add SPI/BPI Flash...
- Boot from Configuration Memory Device
- Assign New Configuration File... **1**
- Set Programming Properties...
- Readback Bit
- Verify Bit

Diagram showing TDI and TDO connections to ps_dap bypass and fmd byp.

TAP_num = 1
IR Length = 4bit

Program setup...

BIT/NKY file: ...

Use customized files

BMM file: ...

ELF file: ...

2 OK Cancel

Warning

A BIT file describing a Unknown is about to be assigned to a device previously identified as a Unknown. Are you sure you want to do this?

3 Yes No

General Device Properties Cable Properties

Boundary Scan X

Console

```
>>init_chain -cable_type jlink
hw_server: Jlink firmware version: 9.70
hw_server: Jlink driver version: 6.50a
hw_server: Select Device Successfully
hw_server: Set Jlink speed to 6000khz failed
hw_server: Current Jlink speed is 65534khz
hw_server: Jlink speed is already 6000khz
hw_server: JTAG tap: Procise found HwServer chain_info: 0x03731093 (mfg:0x049(FMSH), part:0x3731(jfm7z045), ver:0x0)
hw_server: read rsvd_reg_7
hw_server: read rsvd value 0x00000000 !

hw_server: JTAG tap: Procise found HwServer chain_info: 0x4ba00477 (mfg:0x23b(ARM), part:0xba00(arm_dap), ver:0x4)
-----
device_id: 00000011011100110001000010010011
manufacturer: FMSH
part_name: fmq145
part_id: 0
ir_length: 6
version: 0
step_id: 0
-----
device_id: 01001011101000000000010001110111
manufacturer: FMSH
part_name: ps_dap
part_id: 1
ir_length: 4
version: 0
step_id: 0
hw_server: SVF instructions execute success
init_chain elapsed_time 2.77 seconds, cpu_time 0.17 seconds
init_chain used memory 1MB, procise used peak memory 962MB, current used memory 875MB
```

Command>

PROCISE - Program

File View Window Psoc Tools Help

Main

Chain configuration of your board

TDI

TDO

TAP_num = 1 0

IR Length = 4bit 6bit

Cables

Cable	Status
SEGGER_	Connected

General Device Properties Cable Properties

Boundary Scan

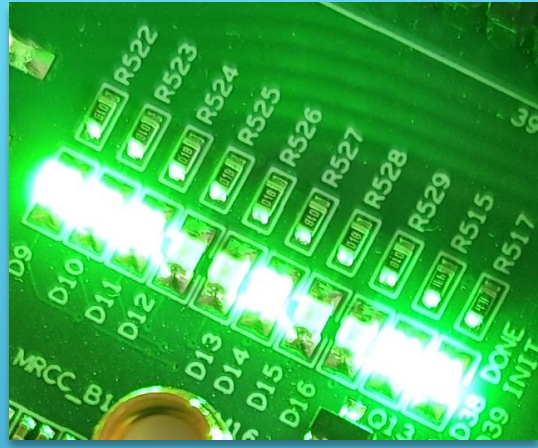
Program Device Succeeded

Console

```

part_name: ps_dap
part_id: 1
ir_length: 4
version: 0
step_id: 0
hw_server: SVF instructions execute success
init_chain elapsed_time 2.77 seconds, cpu_time 0.17 seconds
init_chain used memory 1MB, procise used peak memory 962MB, current used memory 875MB
>>program_bit F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/rundir/led_procise.bit -part 0
hw_server: Accepting 'procise' connection 1772 on top 8888
hw_server: The initial jlink speed is 6000khz, adjust the speed to 12000khz automatically when scan big data
hw_server: Set Jlink speed to 12000khz successfully
hw_server: scan big data finished, set cable speed back to 6000khz
hw_server: Set Jlink speed to 6000khz successfully
BOOTSTS: 0x00000001
STAT: 0x40007ffc
Startup state machine: Phase 5
hw_server: SVF instructions execute success
program_bit elapsed_time 48.40 seconds, cpu_time 3.27 seconds
program_bit used memory 39MB, procise used peak memory 962MB, current used memory 918MB
>>program_bit F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/rundir/led_procise.bit -part 0
hw_server: Accepting 'procise' connection 1824 on top 8888
hw_server: The initial jlink speed is 6000khz, adjust the speed to 12000khz automatically when scan big data
hw_server: Set Jlink speed to 12000khz successfully
hw_server: scan big data finished, set cable speed back to 6000khz
hw_server: Set Jlink speed to 6000khz successfully
BOOTSTS: 0x00000001
STAT: 0x40007ffc
Startup state machine: Phase 5
hw_server: SVF instructions execute success
program_bit elapsed_time 43.24 seconds, cpu_time 2.94 seconds
program_bit used memory 38MB, procise used peak memory 962MB, current used memory 907MB
Command:

```



ЗАПУСК IAR ЧЕРЕЗ PROCISE 2023.1

The screenshot shows the PROCISE 2023.1 interface. The main window displays the 'led4 Project Status' and 'Utilization' sections. The 'Project Status' section shows the project file 'led4.fpe', module name 'system_wrapper', target device 'fmq145t900', and product version 'Procise 2023.1'. The 'Utilization' section shows a summary table with 234 instances, 4 LUTs, 0 FFs, 0 CUs, and 0 RAMB. Below this is a 'Plot' section showing slice LUTs at 4/218600 (0.00%) and bonded IOUs at 4/362 (1.10%).

Instances	LUTs	FFs	CUs	RAMB
234	4	0	0	0

Category	Total Used	Type	Used
LCs	3	LCL	3
		ILGKE3	4
		IOINF	130
		IOU33	4
Others	231	OLGKE3	4

The 'Export Hardware...' menu item is highlighted with a red box. Below it, the text 'Запуск компиляции библиотек и выбор шаблонов для программы' and 'Запуск IAR 8.11.2' is written in red.

The TCL Console at the bottom shows the following output:

```
set_device elapsed_time 0.00 seconds, cpu_time 0.00 seconds
set_device used memory 892MB, procise used peak memory 962MB, current used memory 709MB

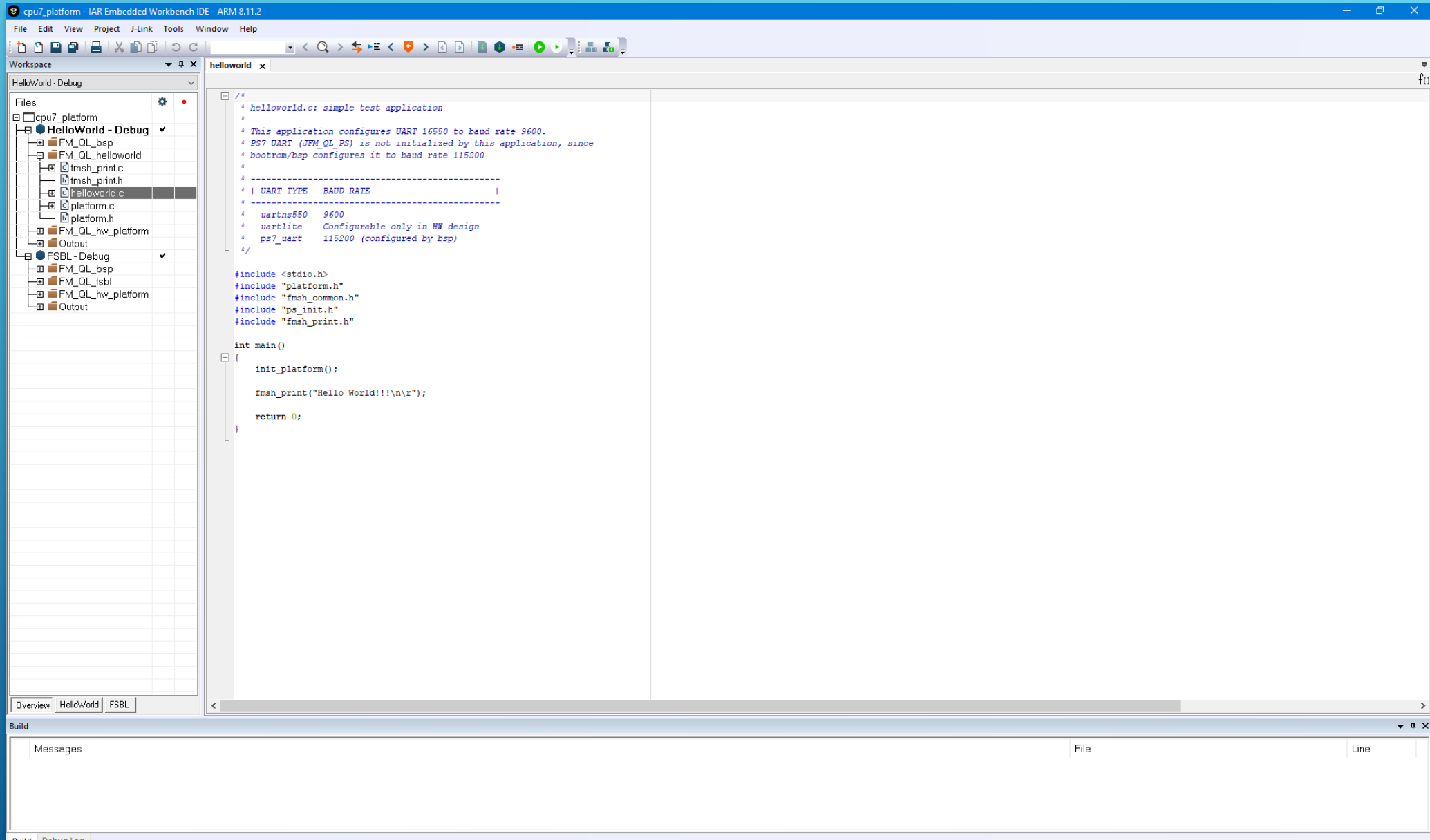
Instance system_i in Module system_wrapper is not defined!
>>load_design -stage_post_map -no_hier
Instance system_i in Module system_wrapper is not defined!
-- Analyzing Verilog file 'F:/_WORK2/_HYPERCUBE/pcie/my_demo/ch3_led4/led4/bd/system/hdl/system.v' (VERI-1482)
-- Analyzing Verilog file 'F:/_WORK2/_HYPERCUBE/pcie/my_demo/ch3_led4/led4/bd/system/hdl/system_wrapper.v' (VERI-1482)
read_phy_design F:/_WORK2/_HYPERCUBE/pcie/my_demo/ch3_led4/led4/rundir/.83ea5c0ce21ff26e3879e961ff2c9278.phy
Read FDC F:/_WORK2/_HYPERCUBE/pcie/my_demo/ch3_led4/led4/rundir/system_wrapper_placed.fdc
load_design elapsed_time 0.70 seconds, cpu_time 0.83 seconds
load_design used memory 11MB, procise used peak memory 962MB, current used memory 724MB
```

The screenshot shows the 'Export Hardware Project' dialog box. The 'Select Project Type' section has several options with checkboxes:

- Empty
- FSBL
- MemoryTest
- PUFGen
- PeripheralTest
- Lwip
- SdFats
- HelloWorld
- DDR3Test
- Efuse
- FlashLoader
- DeviceTree
- FreeRTOS

The 'OK' and 'Cancel' buttons are visible at the bottom of the dialog box.

IAR 8.11.2





Workspace

Files

- cpu7_platform
 - HelloWorld - Debug**
 - FM_QL_bsp
 - FM_QL_helloworld
 - fmsh_print.c
 - fmsh_print.h
 - helloworld.c
 - platform.c
 - platform.h
 - FM_QL_hw_platform
 - Output
 - FSBL - Debug
 - FM_QL_bsp
 - FM_QL_fsbl
 - FM_QL_hw_platform
 - Output

helloworld x

```

main()
/*
 * helloworld.c: simple test application
 *
 * This application configures UART 16550 to baud rate 9600.
 * PS7 UART (JFM_QL_PS) is not initialized by this application, since
 * bootrom/bsp configures it to baud rate 115200
 *
 * -----
 * | UART TYPE   BAUD RATE |
 * -----
 * uarts550     9600
 * uartlite     Configurable only in HW design
 * ps7_uart     115200 (configured by bsp)
 *
 */

#include <stdio.h>
#include "platform.h"
#include "fmsh_common.h"
#include "ps_init.h"
#include "fmsh_print.h"

int main()
{
    init_platform();

    fmsh_print("Hello World!!!\n\r");

    return 0;
}

```

Disassembly

Go to Memory

```

Disassembly
0x1fe28a0: 0x72207472
0x1fe28a4: 0x6f736165
0x1fe28a8: 0x7369206e
0x1fe28ac: 0x7325203a
0x1fe28b0: 0x000000a

?main:
__cmain:
0x1fe28b4: 0xe3a00001
0x1fe28b8: 0xfa000008
0x1fe28bc: 0xe3500000
0x1fe28c0: 0x0a000000
0x1fe28c4: 0xfaffffb7
__call_main:
0x1fe28c8: 0xe3a00000
0x1fe28cc: 0xe320f000
_main:
0x1fe28d0: 0xeb000003
0x1fe28d4: 0xfa00000b
0x1fe28d8: 0xfaffff64
0x1fe28dc: 0xeafffffd
__low_level_init:
0x1fe28e0: 0x2001
0x1fe28e2: 0x4770

int main()
{
main:
0x1fe28e4: 0xe92d5000
    init_platform();
0x1fe28e8: 0xebffff11
    fmsh_print("Hello World
0x1fe28ec: 0xe59f0008
0x1fe28f0: 0xebfffd84
    return 0;
0x1fe28f4: 0xe3a00000
0x1fe28f8: 0xe8bd8002
0x1fe28fc: 0xe1fe2b7c
?Veneer (6) for __exit:
0x1fe2900: 0xf8df 0xf00
0x1fe2904: 0xe1fe290c
exit:
0x1fe2908: 0xf7ff 0xbff
__exit:
0x1fe290c: 0xe1b07000
0x1fe2910: 0xe1b00007
0x1fe2914: 0xfaffff55
0x1fe2918: 0xeafffffd
    iar copy init3:

```

Debug Log

```

Log
Tue Apr 23, 2024 15:55:00: Found 2 JTAG devices, Total IRLen = 10:
Tue Apr 23, 2024 15:55:00: #0 Id: 0x03731093, IRLen: 6, Unknown device
Tue Apr 23, 2024 15:55:00: #1 Id: 0x4BA00477, IRLen: 4, IRPrint: 0x1 CoreSight JTAG-DP
Tue Apr 23, 2024 15:55:00: 16328 bytes downloaded (53.69 Kbytes/sec)
Tue Apr 23, 2024 15:55:00: Loaded debuggee: F:\WORK2\FUDAN\golden_demo\ch0_helloworld\hello\SDK\cpu7_platform\HelloWorld\Debug\Exe\HelloWorld.out
Tue Apr 23, 2024 15:55:00: Software reset was performed
Tue Apr 23, 2024 15:55:00: Target reset

```


ВЫВОД СООБЩЕНИЙ СТАРТОВОГО ЗАГРУЗЧИКА

```
====PSOC FSBL BOOTING ..... ==== // Загрузка загрузчика 1го этапа
====FSBL Version: 3.24 ====
====Procise SVN Version: 28852 Release Date: 2023/06/26 15:21:15====
===== In BootStage 1 ===== // 1й этап загрузки
====UART initialized success!!!====
BootMode Register is : 0x00000141
PS was reset by Non_POR!!! // Загрузка по кнопке PS_RST_B
PS was booted nonsecurely last time,Non Secure mode is set! // небезопасная загрузка
Cluster ID 0x13731093
Running on A7-0
Boot Initialize is done at the 32.78 ms
===== In BootStage 2 ===== // 2-й этап загрузки
Preparing boot device initialization..... // Загрузка через QSPI
QSPI Boot Mode
Boot device initialization success.....
Boot device initialization is done at the 49.27 ms
Preparing boot header search and validate..... // Поиск заголовка и проверка
Multiboot register: 0x0
Image start address: 0x0
Load boot header info (offset:0x20~0x48)success! // загрузка заголовка
Image ID verified success!!! // совпадение ИД образа
Checksum verified success!!! // совпадение КС
```

```
Boot header validate success, this is a valid image!!! // успешно проверен заголовок образа
Boot header search is done at the 76.88 ms
Image Header Table Offset 0x8c0 // загрузка таблицы заголовков образов
Checksum verified success!!! // проверка КС успешна
Checksum validate success!!! // совпадение КС
Image Header Table Details // Таблица заголовков образов
Boot Gen Ver: 0x1020000
Number of Partitions: 0x3
Partition Header Address: 0x270
Partition Present Device: 0x0
Boot header validate is done at the 101.72 ms
===== In BootStage 3 =====
Partition header validate.....
Checksum verified success!!!
Partition is unencrypted.....
Partition is unauthenticated.....
UnEncrypted data Length: 0x32d15c
Data word offset: 0x32d15c
Total Data word length: 0x32d15c
Destination Load Address: 0xffffffff
Execution Address: 0x0
Data word offset: 0x7e40
Partition Attributes: 0x20
Partition header validate SUCCESS!!
Partition header validate is done at the 142.33 ms
Prepare Copy Partition.....
Copy Partition is done at the 149.45 ms
Prepare downloading bitstream.....
Reduce csu frequency to 29.17Mhz!!!
Recover csu frequency to 83.33Mhz!!!
```

```
Download the PL bitstream is done at the 1257.20 ms
Partition Load Success
===== In BootStage 3 =====
Partition header validate.....
Checksum verified success!!!
Partition is unencrypted.....
Partition is unauthenticated.....
UnEncrypted data Length: 0xff9
Data word offset: 0xff9
Total Data word length: 0xff9
Destination Load Address: 0xe1fe0000
Execution Address: 0xe1fe21d0
Data word offset: 0x334fa0
Partition Attributes: 0x118
Partition header validate SUCCESS!!
Partition header validate is done at the 1300.60 ms
Prepare Copy Partition.....
Copy Partition success!!
Copy Partition is done at the 1311.32 ms
Download the Application is done at the 1314.97 ms
Partition Load Success
All Partitions Loaded
===== In BootStage 4 =====
Handoff control to JTAG or FSBL.....
APU will jump to app or wait for event!!!
Exit from FSBL
Hello World
```