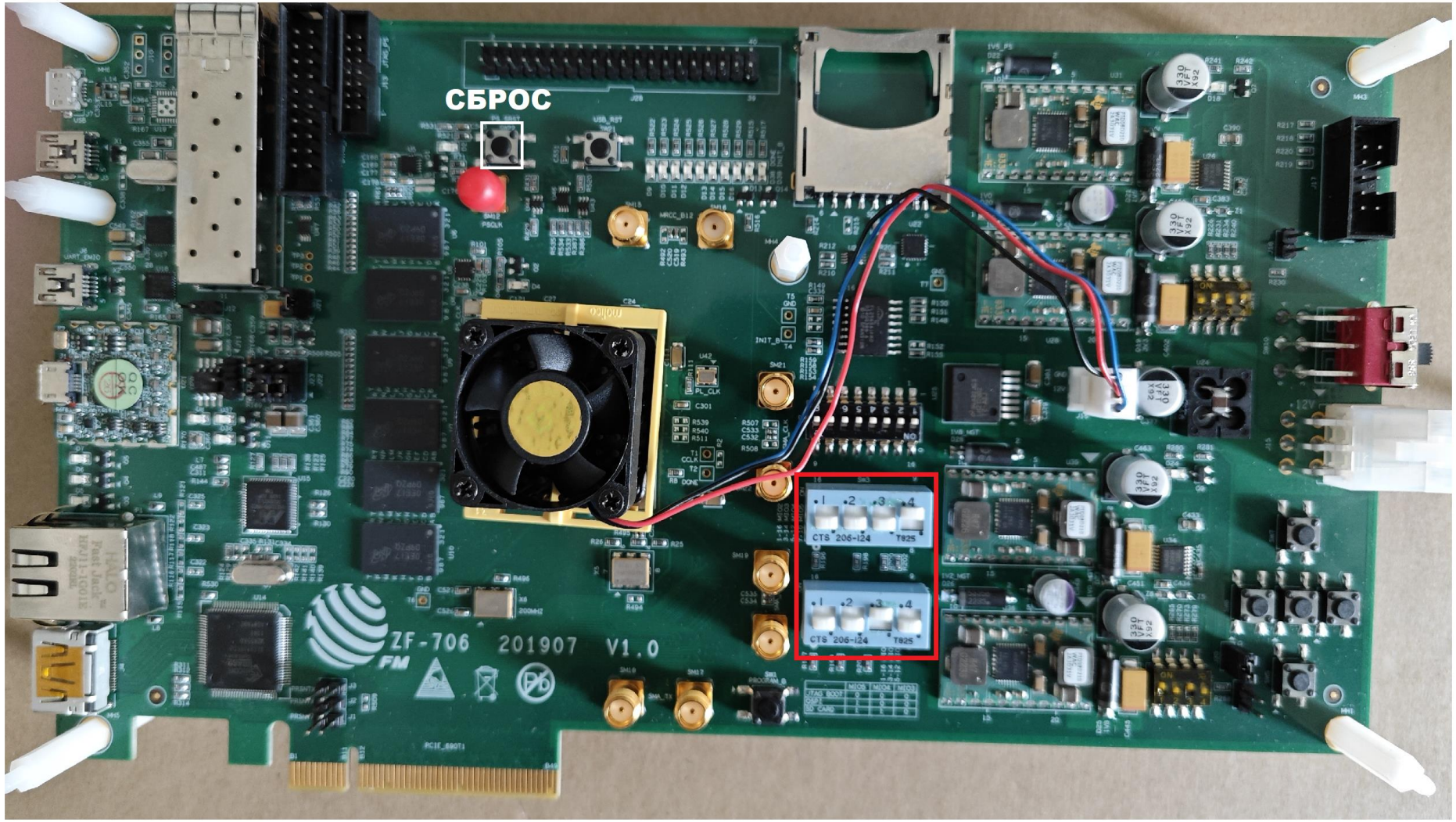
РАБОТА С ОТЛАДОЧНОЙ ПЛАТОЙ ZF-706

на основе ПЛИС Fudan FMQL45T900

СОСТАВ ОТЛАДОЧНОЙ ПЛАТЫ ZF-706

- Fudan FMQL45T900 (4xCortex-A7, 256Кб L2, 256Кб SRAM, 218k LUTs, 437k FFs, 19,2 Мбит BRAM, 900 MACC18x25, 2 ADC)
- Конфигурационное ПЗУ QSPI 256 Мбит
- Генераторы 50 МГц(PS), 33 МГц(PL)
- 1 Гбайт DDR3-1066 PS, 2 Гбайт DDR3-1066 PL
- 1Gb Ethernet (PHY LAN88E1116 RGMII)
- HDMI-выход (1080p @ 60 Гц)
- USB-UART PS(CP2102), USB-UART EMIO (CP2102), USB2.0(USB3320C)
- Интерфейс SD-card
- Интерфейс PCIe x8
- Встроенный программатор USB-JTAG (совместим с Digilent)

ВНЕШНИЙ ВИД ОТЛАДОЧНОЙ ПЛАТЫ ZF-706



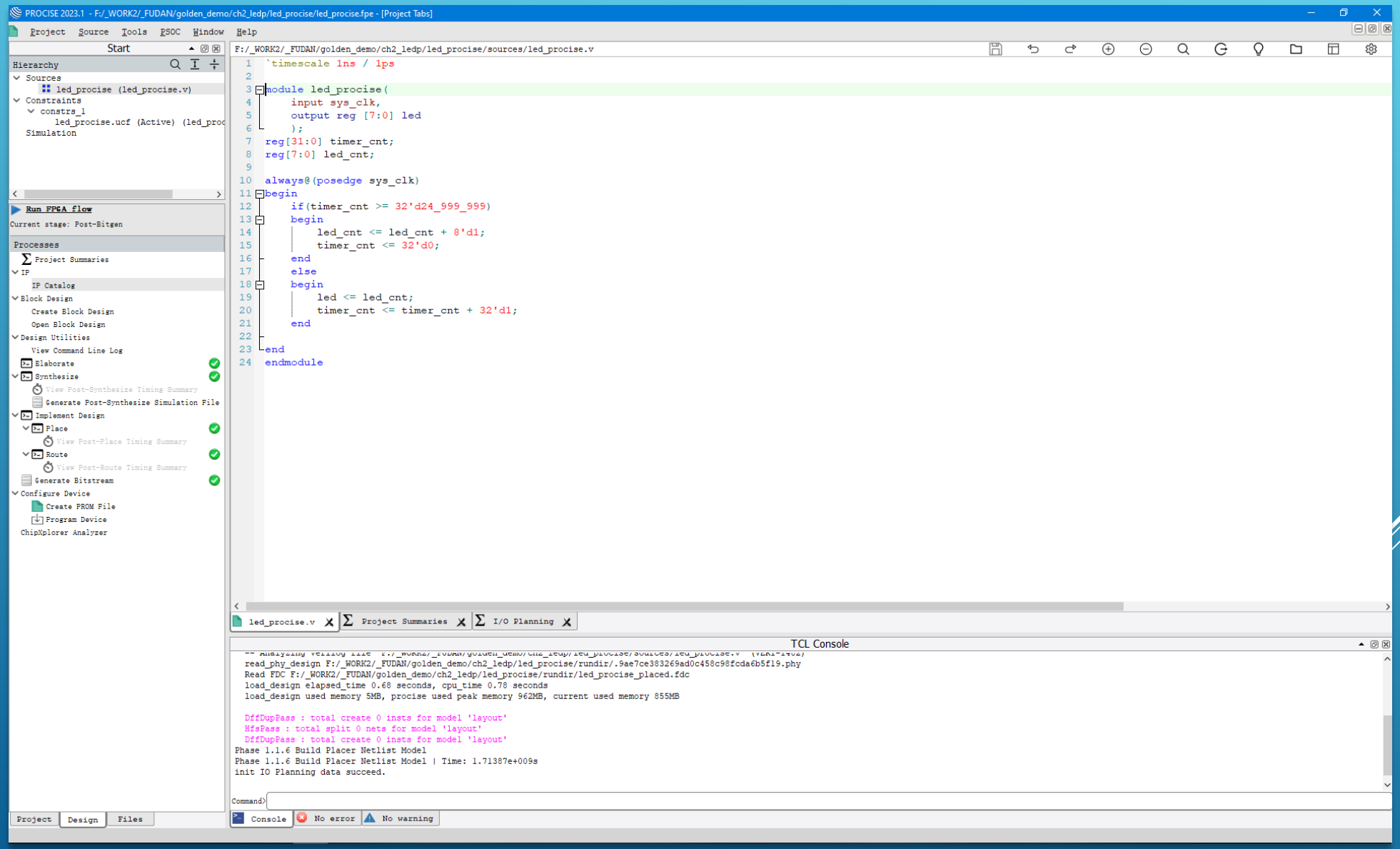
ОСОБЕННОСТИ ПЛИС FMQL45T900

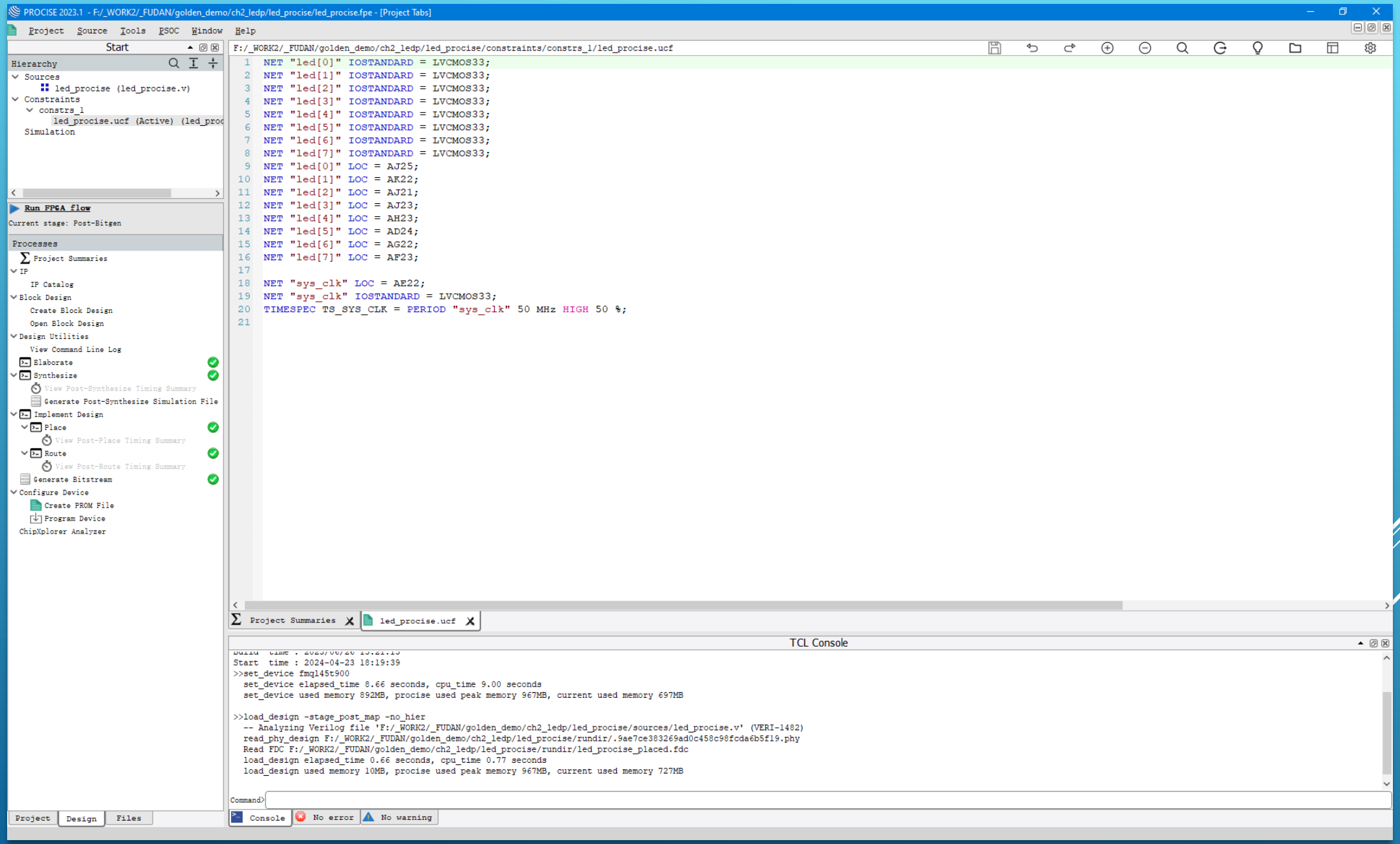
- Необходимость учитывать перенос некоторых сигналов на другие выводы и межсоединения относительно аналога Xilinx (SD_CDn, SRAM_BLS_B, CPU_IRQ)
- Отсутствие арбитража и управления потоком (handshake/flow control) DMA-транзакций между PS и PL
- Необходимость учитывать отличия в DDR-контроллере (контакты VRN/VRP)
- 4 ядра ARM Cortex-A7 вместо 2-х Cortex-A9
- Кэш L2 объемом 256 Кбайт вместо 512 Кбайт
- Работа с СнК в САПР Procise 2023.1 и IAR Embedded Workbench for ARM 8.11.2
- Работа с ПЛИС в САПР Procise 2023.1 или Vivado 2018.3
- Необходимость учитывать особенности ПЛИС при работе в Vivado 2018.3

ОСОБЕННОСТИ РАБОТЫ С ОТЛАДОЧНОЙ ПЛАТОЙ

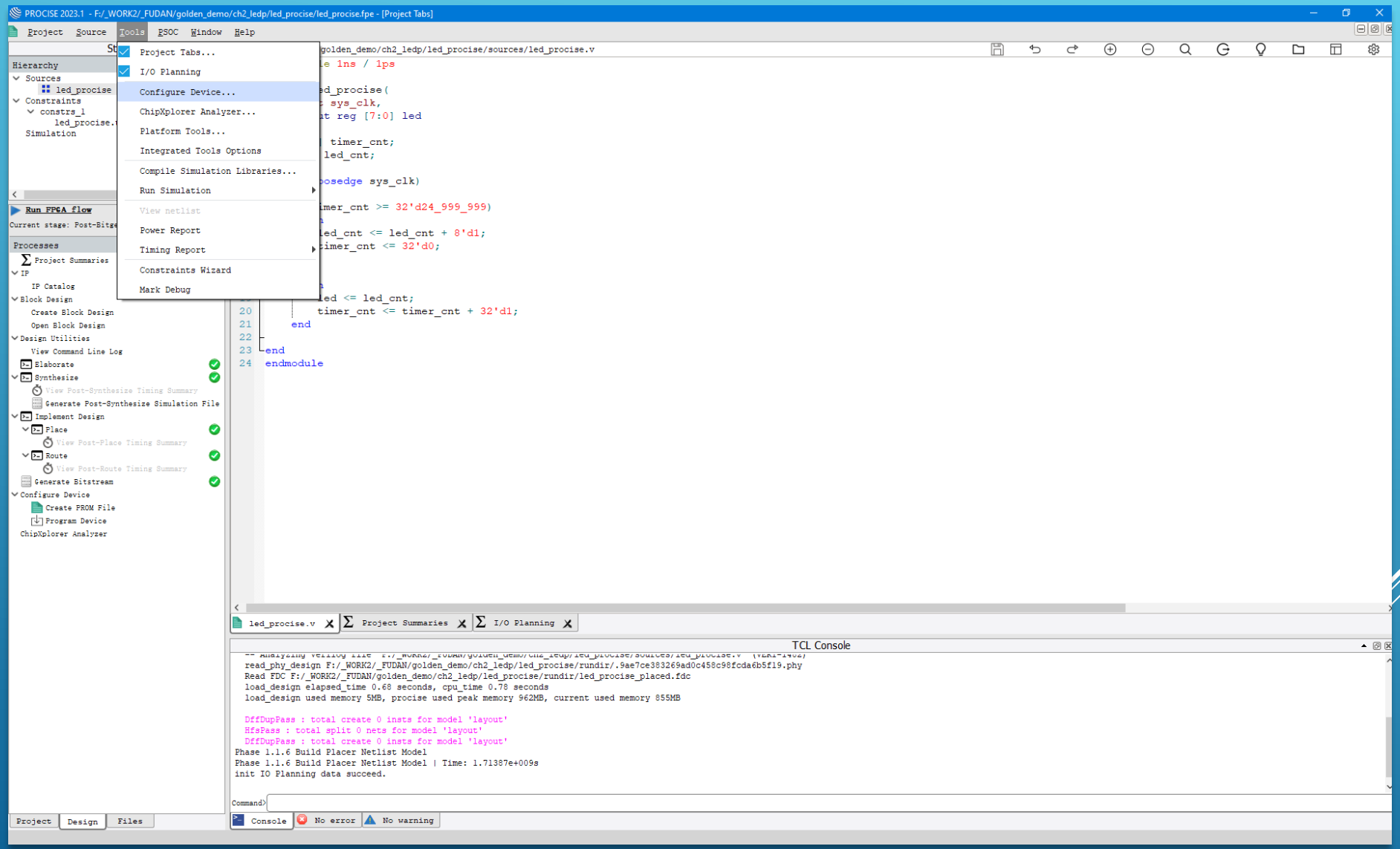
- Работа в Vivado 2018.3 с ПЛИС осуществляется через Digilent-совместимый программатор распаянный на плате (JTAG PL)
- Работа с СнК и ПЛИС в Procise 2023.1 и IAR 8.2.11 осуществляется через программатор J-link V9 (Jlink firmware ver. 9.70; Jlink driver ver. 6.50a)
- При отладке проекта в IAR необходимо переводить СнК в режим загрузки через JTAG, иначе СнК будет загружаться с SD/QSPI, что приведет к конфликту при отладке
- В начале работы необходимо проверить и правильно выставить перемычки (джамперы) и микропереключатели согласно описанию на отладочную плату

PROGRAMMABLE CIRCUIT AND SYSTEM COMPILER (PROCISE 2023.1)

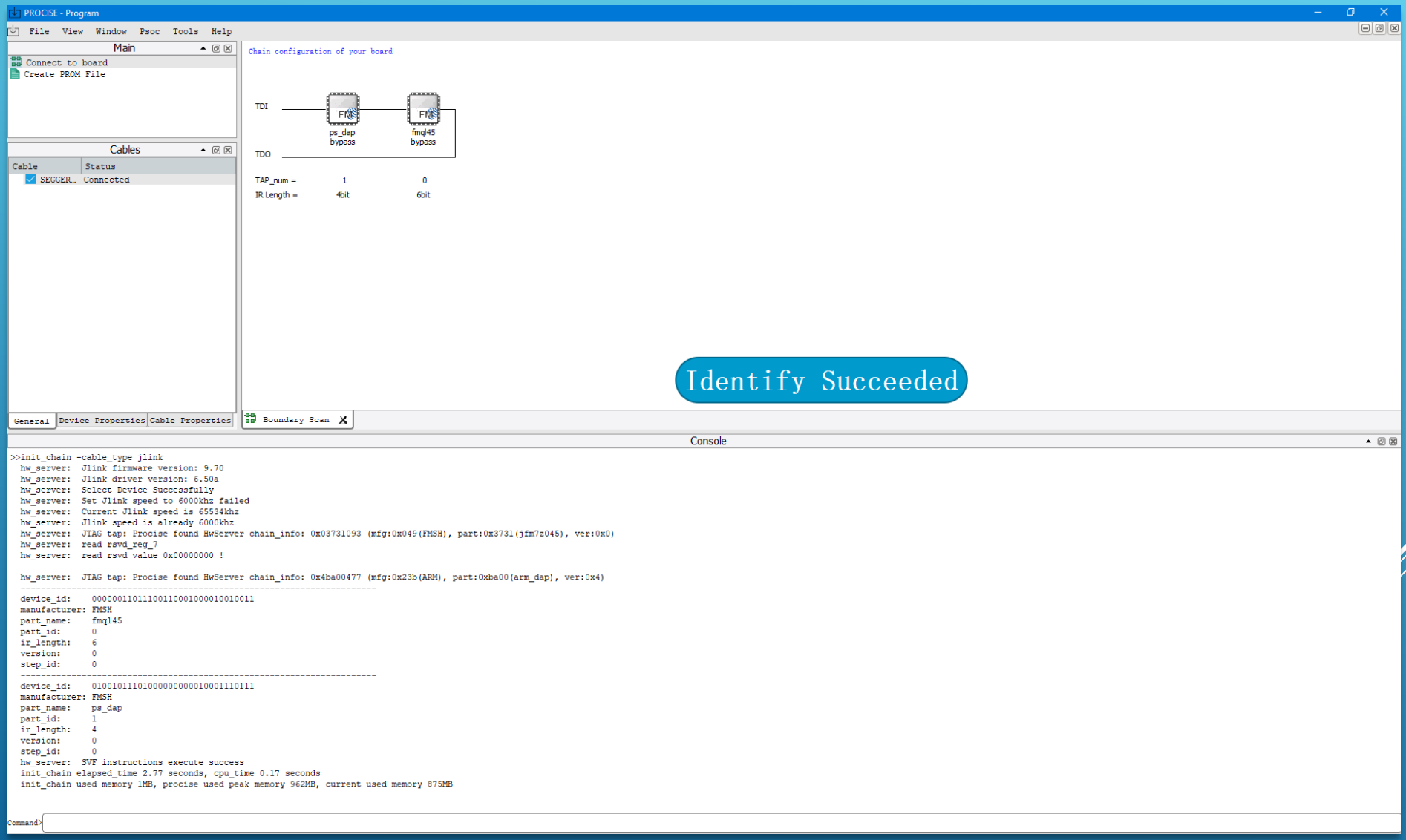


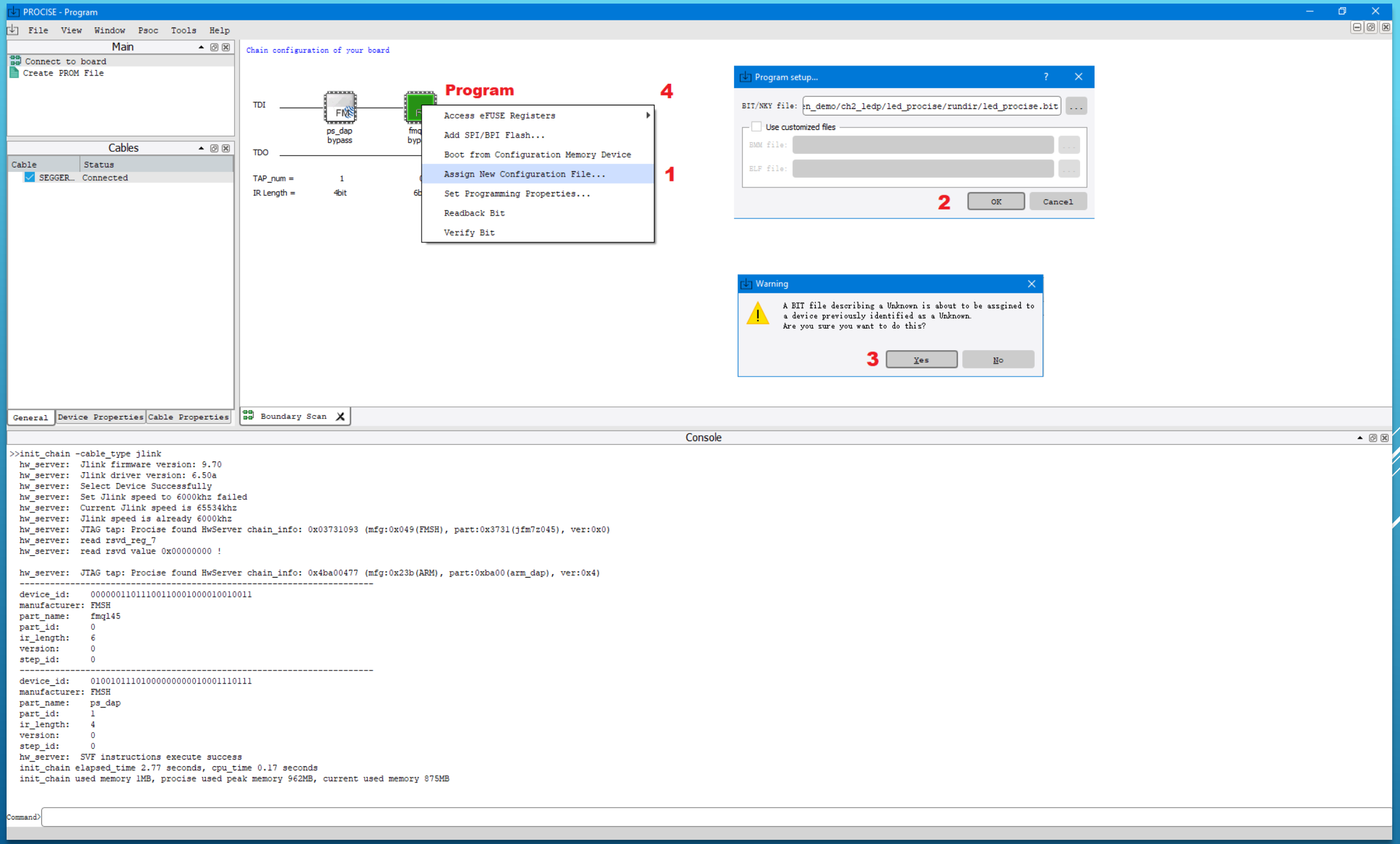

PROCISE 2023.1 - F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/led_procise.fpe - [Project Tabs]
Project Source Tools PSOC Window Help
Start
Hierarchy
Sources
led_procise (led_procise.v)
Constraints
constrs_1
led_procise.ucf (Active) (led_proc
Simulation
Run FPGA flow
Current stage: Post-Bitgen
Processes
Project Summaries
IP
IP Catalog
Block Design
Create Block Design
Open Block Design
Design Utilities
View Command Line Log
Elaborate
Synthesize
View Post-Synthesize Timing Summary
Generate Post-Synthesize Simulation File
Implement Design
Place
View Post-Place Timing Summary
Route
View Post-Route Timing Summary
Generate Bitstream
Configure Device
Create PROM File
Program Device
ChipXplorer Analyzer
Project
Design
Files
F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/constraints/constrs_1/led_procise.ucf
1 NET "led[0]" IOSTANDARD = LVCMOS33;
2 NET "led[1]" IOSTANDARD = LVCMOS33;
3 NET "led[2]" IOSTANDARD = LVCMOS33;
4 NET "led[3]" IOSTANDARD = LVCMOS33;
5 NET "led[4]" IOSTANDARD = LVCMOS33;
6 NET "led[5]" IOSTANDARD = LVCMOS33;
7 NET "led[6]" IOSTANDARD = LVCMOS33;
8 NET "led[7]" IOSTANDARD = LVCMOS33;
9 NET "led[0]" LOC = AJ25;
10 NET "led[1]" LOC = AK22;
11 NET "led[2]" LOC = AJ21;
12 NET "led[3]" LOC = AJ23;
13 NET "led[4]" LOC = AH23;
14 NET "led[5]" LOC = AD24;
15 NET "led[6]" LOC = AG22;
16 NET "led[7]" LOC = AF23;
17
18 NET "sys_clk" LOC = AE22;
19 NET "sys_clk" IOSTANDARD = LVCMOS33;
20 TIMESPEC TS_SYS_CLK = PERIOD "sys_clk" 50 MHz HIGH 50 %;
21
Project Summaries
led_procise.ucf
TCL Console
Start time : 2024-04-23 18:19:39
>>set_device fmq145t900
set_device elapsed_time 8.66 seconds, cpu_time 9.00 seconds
set_device used memory 892MB, procise used peak memory 967MB, current used memory 697MB
>>load_design -stage_post_map -no_hier
-- Analyzing Verilog file 'F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/sources/led_procise.v' (VERI-1482)
read_phy_design F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/rundir/.9ae7ce383269ad0c458c98fcda6b5f19.phy
Read FDC F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/rundir/led_procise_placed.fdc
load_design elapsed_time 0.66 seconds, cpu_time 0.77 seconds
load_design used memory 10MB, procise used peak memory 967MB, current used memory 727MB
Command>
Console
No error
No warning

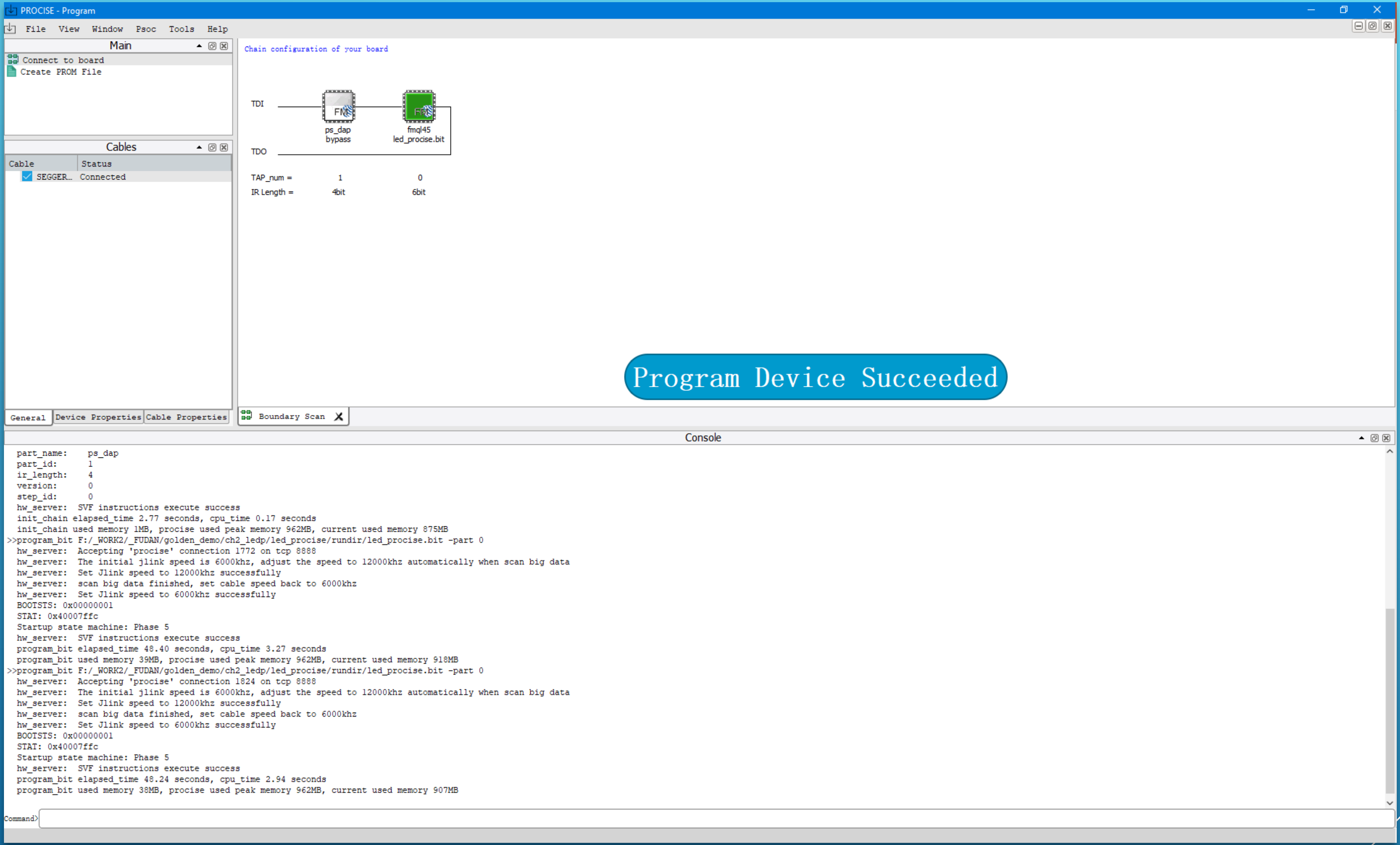
ЗАГРУЗКА ПРОГРАММЫ В ПЛИС ЧЕРЕЗ JTAG

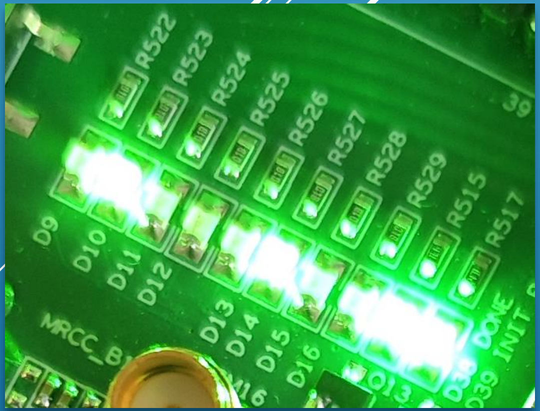


ЗАГРУЗКА ПРОГРАММЫ В ПЛИС ЧЕРЕЗ JTAG

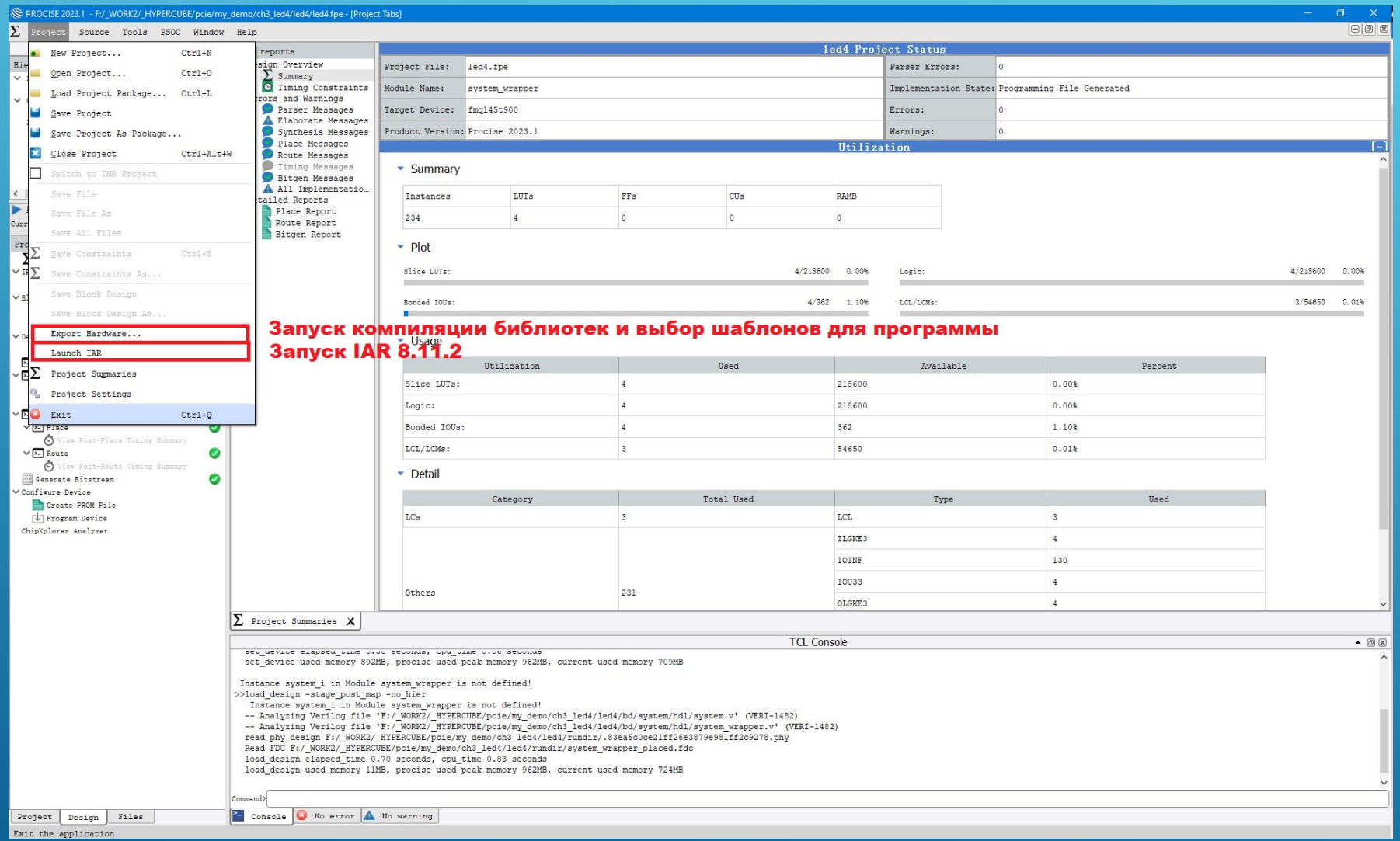


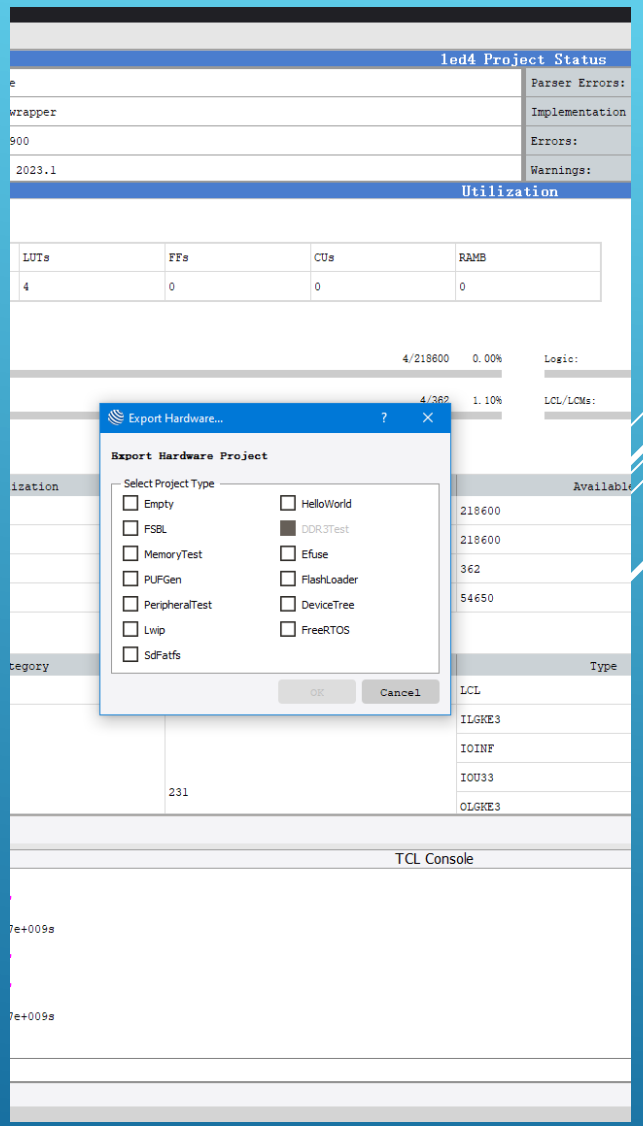

PROCISE - Program
File View Window Psoc Tools Help
Main
Connect to board
Create PROM File
Cables
Cable Status
SEGGER... Connected
General Device Properties Cable Properties
Chain configuration of your board
TDI
TDO
TAP_num = 1
IR Length = 4bit
ps_dap bypass
Program
4
Access eFUSE Registers
Add SPI/BPI Flash...
Boot from Configuration Memory Device
Assign New Configuration File...
1
Set Programming Properties...
Readback Bit
Verify Bit
Program setup...
BIT/NKY file: n_demo/ch2_ledp/led_procise/rundir/led_procise.bit
Use customized files
BMM file:
BLF file:
2
OK
Cancel
Warning
A BIT file describing a Unknown is about to be assgined to a device previously identified as a Unknown.
Are you sure you want to do this?
3
Yes
No
Boundary Scan
Console
>>init_chain -cable_type jlink
hw_server: Jlink firmware version: 9.70
hw_server: Jlink driver version: 6.50a
hw_server: Select Device Successfully
hw_server: Set Jlink speed to 6000khz failed
hw_server: Current Jlink speed is 65534khz
hw_server: Jlink speed is already 6000khz
hw_server: JTAG tap: Procise found HwServer chain_info: 0x03731093 (mfg:0x049(FMSH), part:0x3731(jfm7z045), ver:0x0)
hw_server: read rsvd_reg_7
hw_server: read rsvd value 0x00000000 !
hw_server: JTAG tap: Procise found HwServer chain_info: 0x4ba00477 (mfg:0x23b(ARM), part:0xba00(arm_dap), ver:0x4)
device_id: 00000011011100110001000010010011
manufacturer: FMSH
part_name: fmql45
part_id: 0
ir_length: 6
version: 0
step_id: 0
device_id: 01001011101000000000010001110111
manufacturer: FMSH
part_name: ps_dap
part_id: 1
ir_length: 4
version: 0
step_id: 0
hw_server: SVF instructions execute success
init_chain elapsed_time 2.77 seconds, cpu_time 0.17 seconds
init_chain used memory 1MB, procise used peak memory 962MB, current used memory 875MB
Command>


PROCISE - Program
File View Window Psoc Tools Help
Main
Connect to board
Create PROM File
Cables
Cable Status
SEGGER... Connected
General Device Properties Cable Properties
Chain configuration of your board
TDI
TDO
ps_dap
bypass
fmql45
led_procise.bit
TAP_num = 1 0
IR Length = 4bit 6bit
Program Device Succeeded
Boundary Scan
Console
part_name: ps_dap
part_id: 1
ir_length: 4
version: 0
step_id: 0
hw_server: SVF instructions execute success
init_chain elapsed_time 2.77 seconds, cpu_time 0.17 seconds
init_chain used memory 1MB, procise used peak memory 962MB, current used memory 875MB
>>program_bit F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/rundir/led_procise.bit -part 0
hw_server: Accepting 'procise' connection 1772 on tcp 8888
hw_server: The initial jlink speed is 6000khz, adjust the speed to 12000khz automatically when scan big data
hw_server: Set Jlink speed to 12000khz successfully
hw_server: scan big data finished, set cable speed back to 6000khz
hw_server: Set Jlink speed to 6000khz successfully
BOOTSTS: 0x00000001
STAT: 0x40007ffc
Startup state machine: Phase 5
hw_server: SVF instructions execute success
program_bit elapsed_time 48.40 seconds, cpu_time 3.27 seconds
program_bit used memory 39MB, procise used peak memory 962MB, current used memory 918MB
>>program_bit F:/_WORK2/_FUDAN/golden_demo/ch2_ledp/led_procise/rundir/led_procise.bit -part 0
hw_server: Accepting 'procise' connection 1824 on tcp 8888
hw_server: The initial jlink speed is 6000khz, adjust the speed to 12000khz automatically when scan big data
hw_server: Set Jlink speed to 12000khz successfully
hw_server: scan big data finished, set cable speed back to 6000khz
hw_server: Set Jlink speed to 6000khz successfully
BOOTSTS: 0x00000001
STAT: 0x40007ffc
Startup state machine: Phase 5
hw_server: SVF instructions execute success
program_bit elapsed_time 48.24 seconds, cpu_time 2.94 seconds
program_bit used memory 38MB, procise used peak memory 962MB, current used memory 907MB
Command>

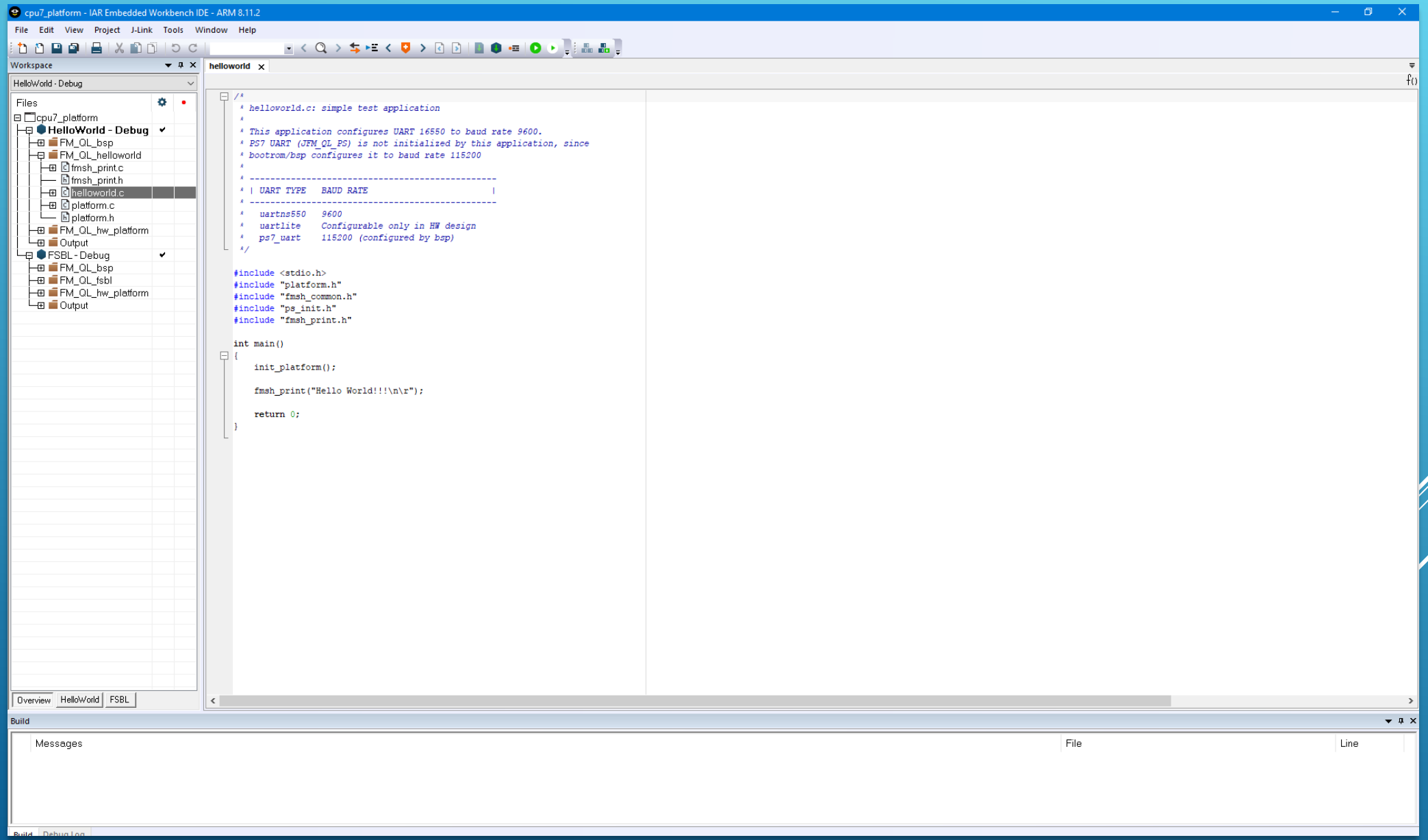


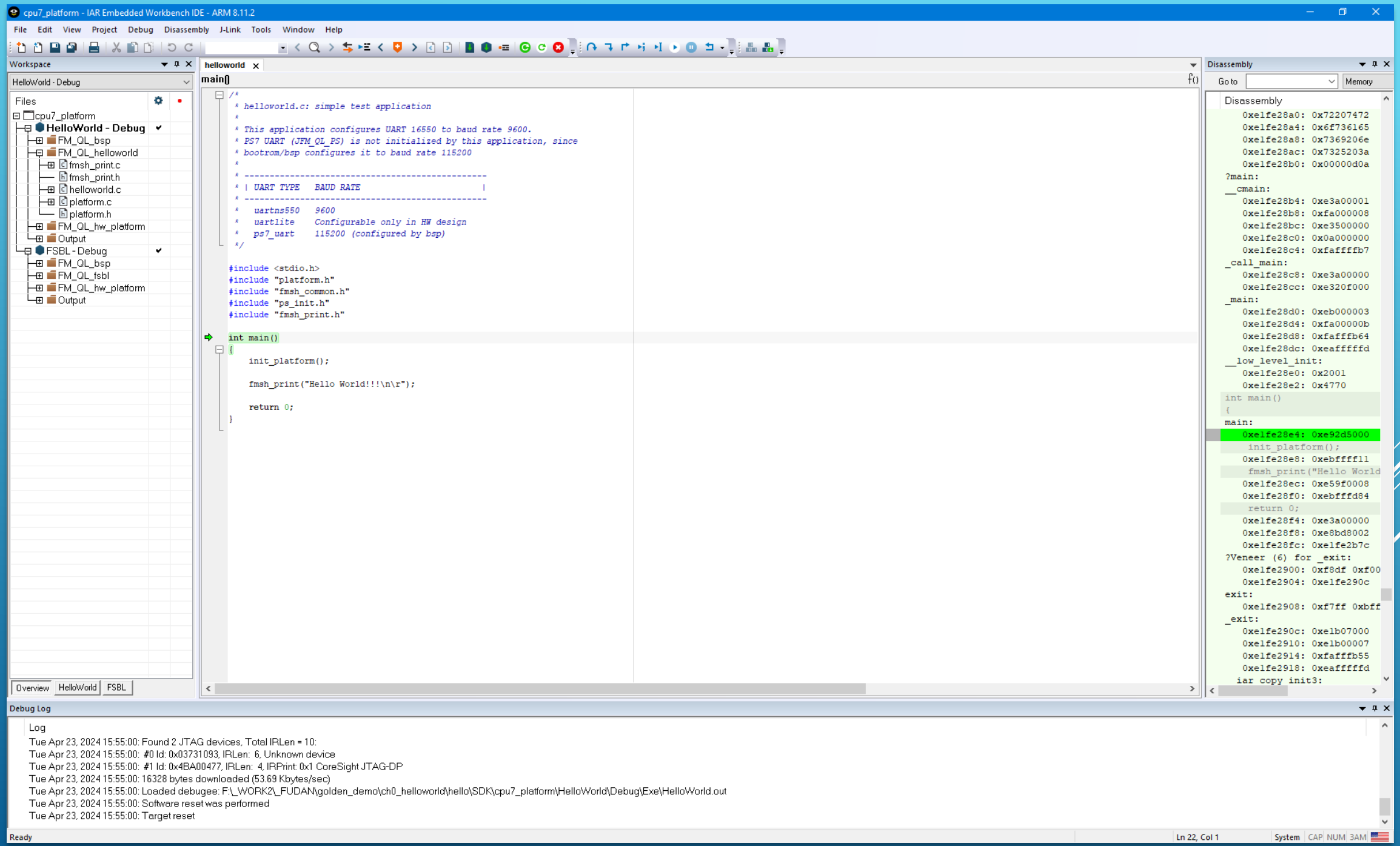
ЗАПУСК IAR ЧЕРЕЗ PROCISE 2023.1





IAR 8.11.2


cpu7_platform - IAR Embedded Workbench IDE - ARM 8.11.2
File Edit View Project J-Link Tools Window Help
Workspace
HelloWorld - Debug
Files
cpu7_platform
HelloWorld - Debug
FM_QL_bsp
FM_QL_helloworld
fmsh_print.c
fmsh_print.h
helloworld.c
platform.c
platform.h
FM_QL_hw_platform
Output
FSBL - Debug
FM_QL_bsp
FM_QL_fsbl
FM_QL_hw_platform
Output
Overview HelloWorld FSBL
helloworld
/*
* helloworld.c: simple test application
*
* This application configures UART 16550 to baud rate 9600.
* PS7 UART (JFM_QL_PS) is not initialized by this application, since
* bootrom/bsp configures it to baud rate 115200
*
* --
* | UART TYPE BAUD RATE |
* --
* uartns550 9600
* uartlite Configurable only in HW design
* ps7_uart 115200 (configured by bsp)
*/
#include <stdio.h>
#include "platform.h"
#include "fmsh_common.h"
#include "ps_init.h"
#include "fmsh_print.h"
int main()
{
init_platform();
fmsh_print("Hello World!!!\n\r");
return 0;
}
Build
Messages
File
Line


cpu7_platform - IAR Embedded Workbench IDE - ARM 8.11.2
File Edit View Project Debug Disassembly J-Link Tools Window Help
Workspace
HelloWorld - Debug
Files
cpu7_platform
HelloWorld - Debug
FM_QL_bsp
FM_QL_helloworld
fmsh_print.c
fmsh_print.h
helloworld.c
platform.c
platform.h
FM_QL_hw_platform
Output
FSBL - Debug
FM_QL_bsp
FM_QL_fsbl
FM_QL_hw_platform
Output
Overview HelloWorld FSBL
helloworld
main()
/*
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*
* --
* | UART TYPE BAUD RATE |
* --
* uartns550 9600
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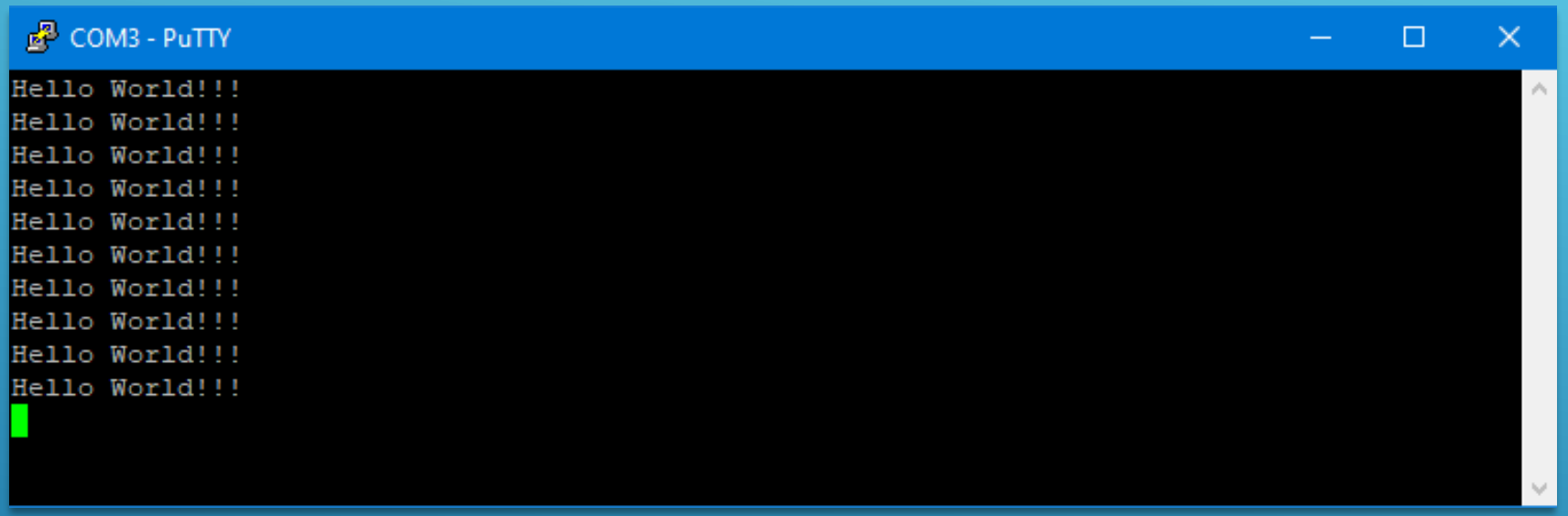
*/
#include <stdio.h>
#include "platform.h"
#include "fmsh_common.h"
#include "ps_init.h"
#include "fmsh_print.h"
int main()
{
init_platform();
fmsh_print("Hello World!!!\n\r");
return 0;
}
Disassembly
Go to
Memory
Disassembly
0xe1fe28a0: 0x72207472
0xe1fe28a4: 0x6f736165
0xe1fe28a8: 0x7369206e
0xe1fe28ac: 0x7325203a
0xe1fe28b0: 0x00000d0a
?main:
__cmain:
0xe1fe28b4: 0xe3a00001
0xe1fe28b8: 0xfa000008
0xe1fe28bc: 0xe3500000
0xe1fe28c0: 0x0a000000
0xe1fe28c4: 0xfaffffb7
_call_main:
0xe1fe28c8: 0xe3a00000
0xe1fe28cc: 0xe320f000
_main:
0xe1fe28d0: 0xeb000003
0xe1fe28d4: 0xfa00000b
0xe1fe28d8: 0xfafffb64
0xe1fe28dc: 0xeafffffd
__low_level_init:
0xe1fe28e0: 0x2001
0xe1fe28e2: 0x4770
int main()
{
main:
0xe1fe28e4: 0xe92d5000
init_platform();
0xe1fe28e8: 0xebffff11
fmsh_print("Hello World
0xe1fe28ec: 0xe59f0008
0xe1fe28f0: 0xebfffd84
return 0;
0xe1fe28f4: 0xe3a00000
0xe1fe28f8: 0xe8bd8002
0xe1fe28fc: 0xe1fe2b7c
?Veneer (6) for _exit:
0xe1fe2900: 0xf8df 0xf00
0xe1fe2904: 0xe1fe290c
exit:
0xe1fe2908: 0xf7ff 0xbff
_exit:
0xe1fe290c: 0xe1b07000
0xe1fe2910: 0xe1b00007
0xe1fe2914: 0xfafffb55
0xe1fe2918: 0xeafffffd
iar copy init3:
Debug Log
Log
Tue Apr 23, 2024 15:55:00: Found 2 JTAG devices, Total IRLen = 10:
Tue Apr 23, 2024 15:55:00: #0 Id: 0x03731093, IRLen: 6, Unknown device
Tue Apr 23, 2024 15:55:00: #1 Id: 0x4BA00477, IRLen: 4, IRPrint: 0x1 CoreSight JTAG-DP
Tue Apr 23, 2024 15:55:00: 16328 bytes downloaded (53.69 Kbytes/sec)
Tue Apr 23, 2024 15:55:00: Loaded debugee: F:_WORK2_FUDAN\golden_demo\ch0_helloworld\hello\SDK\cpu7_platform\HelloWorld\Debug\Exe\HelloWorld.out
Tue Apr 23, 2024 15:55:00: Software reset was performed
Tue Apr 23, 2024 15:55:00: Target reset
Ready
Ln 22, Col 1
System
CAP NUM 3AM


COM3 - PuTTY
Hello World!!!
Hello World!!!
Hello World!!!
Hello World!!!
Hello World!!!
Hello World!!!
Hello World!!!
Hello World!!!
Hello World!!!
Hello World!!!

ВЫВОД СООБЩЕНИЙ СТАРТОВОГО ЗАГРУЗЧИКА

```
====PSOC FSBL BOOTING ..... ====                                  // Загрузка загрузчика 1го этапа
====FSBL Version: 3.24 ====
====Procise SVN Version: 28852  Release Date: 2023/06/26 15:21:15====
======= In BootStage 1 =======                                    // 1й этап загрузки
====UART initialized success!!!====
BootMode Register is : 0x00000141
PS was reset by Non_POR!!!                                        // Загрузка по кнопке PS_RST_B
PS was booted nonsecurely last time,Non Secure mode is set!       // небезопасная загрузка
Cluster ID 0x13731093
Running on A7-0
Boot Initialize is done at the 32.78 ms
======= In BootStage 2 =======                                    // 2-й этап загрузки
Preparing boot device initialization......
QSPI Boot Mode                                                    // Загрузка через QSPI
Boot device  initialization success......
Boot device initialization is done at the 49.27 ms
Preparing boot header search and validate......                   // Поиск заголовка и проверка
Multiboot register: 0x0
Image start address: 0x0
Load boot header info (offset:0x20~0x48)success!                  // загрузка заголовка
Image ID verified success!!!                                      // совпадение ИД образа
Checksum verified success!!!                                      // совпадение КС
```

```
Boot header validate success, this is a valid image!!!     // успешно проверен заголовок образа
Boot header search is done at the 76.88 ms
Image Header Table Offset 0x8c0                            // загрузка таблицы заголовков образов
Checksum verified success!!!                               // проверка КС успешна
Checksum validate success!!!                               // совпадение КС
Image Header Table Details                                 // Таблица заголовков образов
Boot Gen Ver: 0x1020000
Number of Partitions: 0x3
Partition Header Address: 0x270
Partition Present Device: 0x0
Boot header validate is done at the 101.72 ms
======= In BootStage 3 =======
Partition header validate......
Checksum verified success!!!
Partition is unencrypted......
Partition is unauthenticated......
UnEncrypted data Length: 0x32d15c
Data word offset: 0x32d15c
Total Data word length: 0x32d15c
Destination Load Address: 0xffffffff
Execution Address: 0x0
Data word offset: 0x7e40
Partition Attributes: 0x20
Partition header validate SUCCESS!!
Partition header validate is done at the 142.33 ms
Prepare Copy Partition......
Copy Partition is done at the 149.45 ms
Prepare downloading bitstream.....
Reduce csu frequency to 29.17Mhz!!!
Recover csu frequency to 83.33Mhz!!!
```

```
Download the PL bitstream is done at the 1257.20 ms
Partition Load Success
======= In BootStage 3 =======
Partition header validate......
Checksum verified success!!!
Partition is unencrypted......
Partition is unauthenticated......
UnEncrypted data Length: 0xff9
Data word offset: 0xff9
Total Data word length: 0xff9
Destination Load Address: 0xe1fe0000
Execution Address: 0xe1fe21d0
Data word offset: 0x334fa0
Partition Attributes: 0x118
Partition header validate SUCCESS!!
Partition header validate is done at the 1300.60 ms
Prepare Copy Partition......
Copy Partition success!!
Copy Partition is done at the 1311.32 ms
Download the Application is done at the 1314.97 ms
Partition Load Success
All Partitions Loaded
================ In BootStage 4 ============
Handoff control to JTAG or FSBL......
APU will jump to app or wait for event!!!
Exit from FSBL
```

Hello World